

S-series 14.0" Popeye & 15.6" Pebble

UMA/DIS Muxless Schematic

AMD TRINITY APU FS1r2

Thames Pro M2 package

FCH HUDSON M3

REV:1

2012-02-24

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

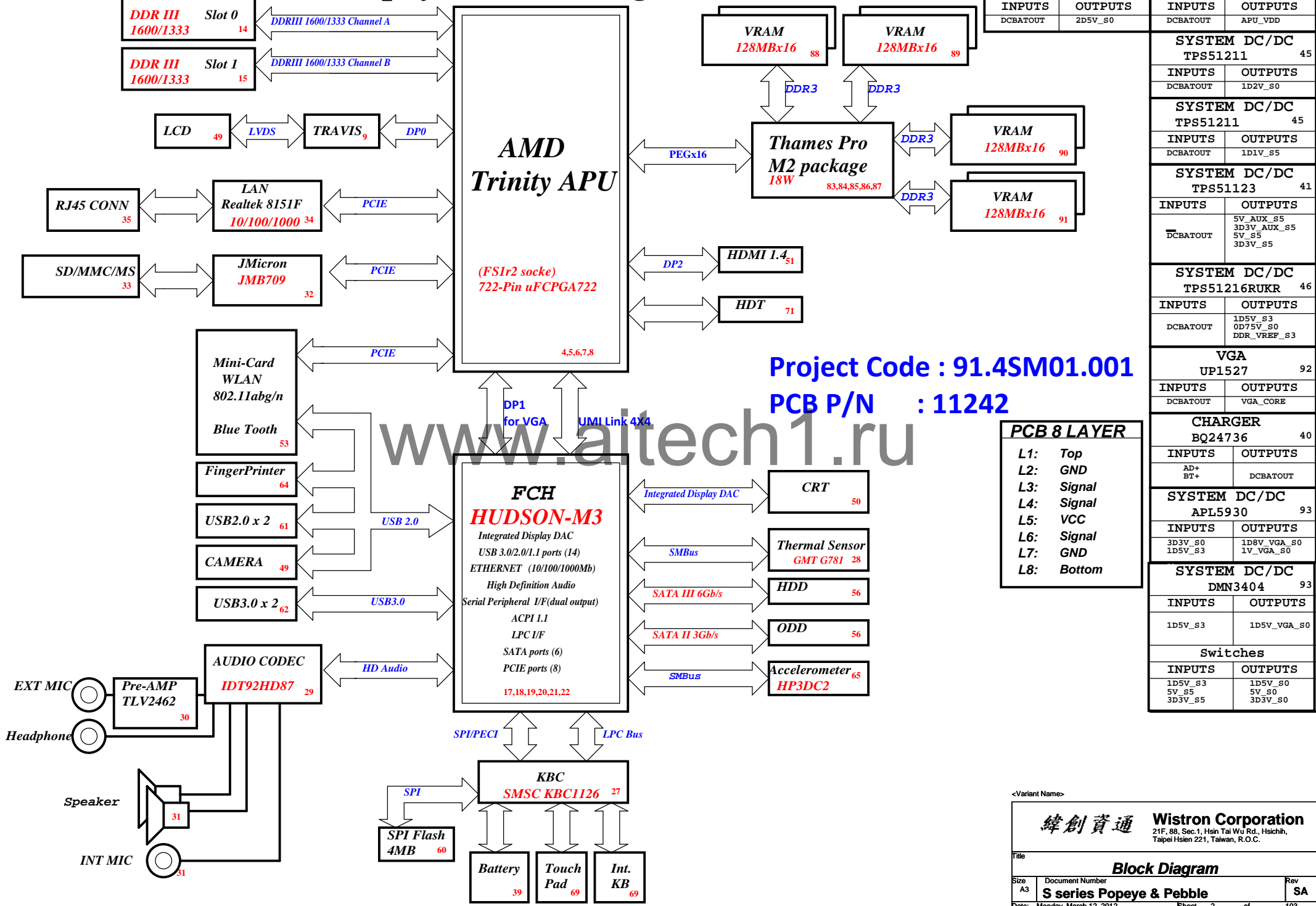
S series Popeye & Pebble

Rev
SA

Date: Monday, March 12, 2012

Sheet 1 of 103

S-series Popeye Block Diagram (Muxless)



S5+ feature

	S0	S3	S5(AC)	S5(DC)		
3D3V_AUX_S5	X	X	X	X	Used	EC
5V_AUX_S5	X	X	X	X	Used	Not used
15V_S5	X	X	X			
5V_S5	X	X	X			
3D3V_S5	X	X	X			
1D1V_S5	X	X	X			
1D5V_S3	X	X				
1D2V_S0	X					
2D5V_S0	X					
0D75V_S0	X					
APU_VDD	X					
APU_VDDNB	X					
5V_S0	X					
3D3V_S0	X					
1D5V_S0	X					
1D1V_S0	X					
3D3V_VGA_S0	X					
VGA_CORE	X					
1V_VGA_S0	X					
1D5V_VGA_S0	X					
1D8V_VGA_S0	X					

USB Table

USB2.0	
Pair	Device
0	USB 2.0 PORT 0 (Right side DB)
1	NA
2	WLAN (WLAN / BT COMBO)
3	USB 2.0 PORT 3 (Right side DB)
4	Camera
5	NA
6	NA
7	NA
8	NA
9	NA
10	NA
11	NA
12	USB 2.0 PORT 12 (USB3.0 CONN)
13	USB 2.0 PORT 13 (USB3.0 CONN)
14	NA
15	FINGER PRINTER


USB3.0	
Pair	Device
0	NA
1	NA
2	USB 3.0 PORT 2
3	USB 3.0 PORT 3

PCIe Routing

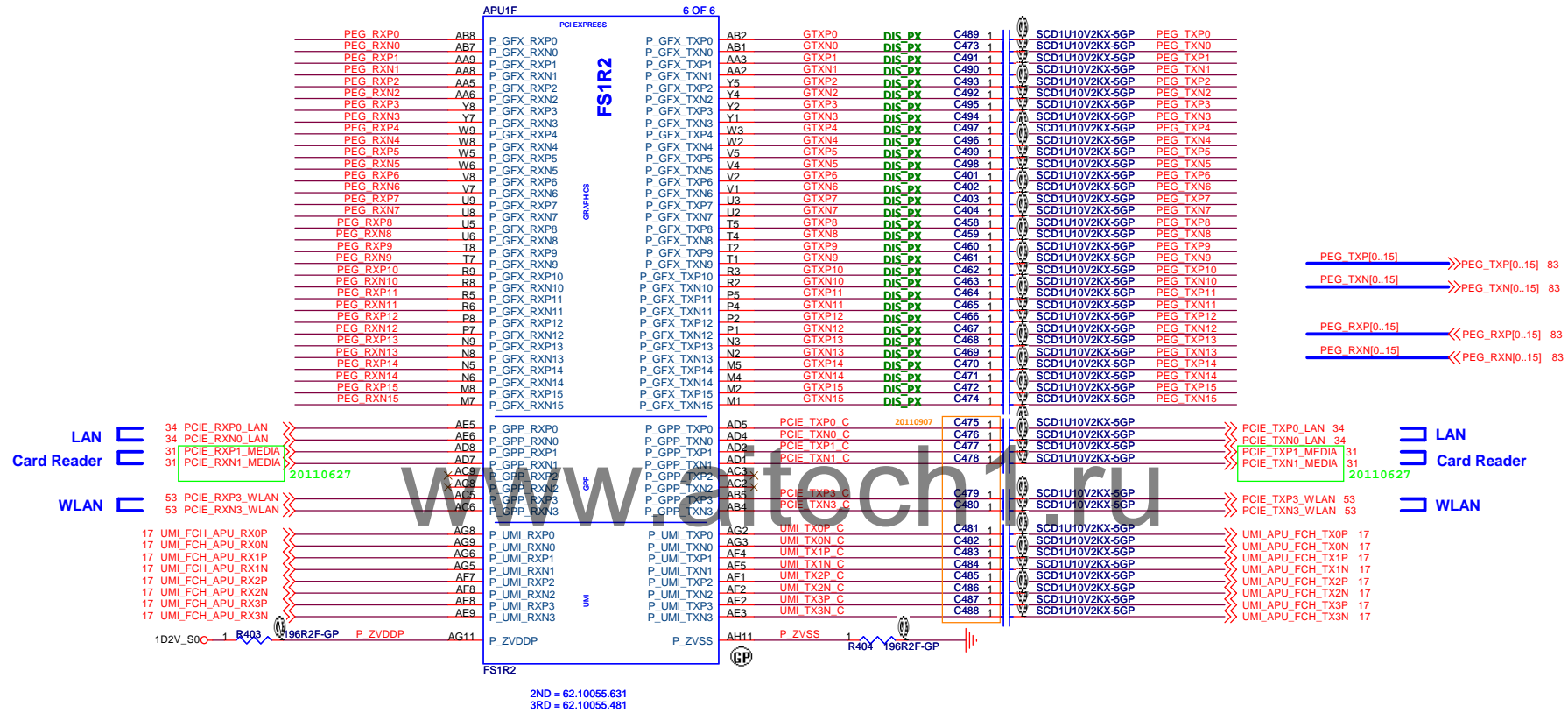
APU PCIE	
LANE0	LAN
LANE1	CardReader
LANE2	NA
LANE3	WLAN

FCH PCIE	
LANE0	NA
LANE1	NA
LANE2	NA
LANE3	NA

<Variant Name>

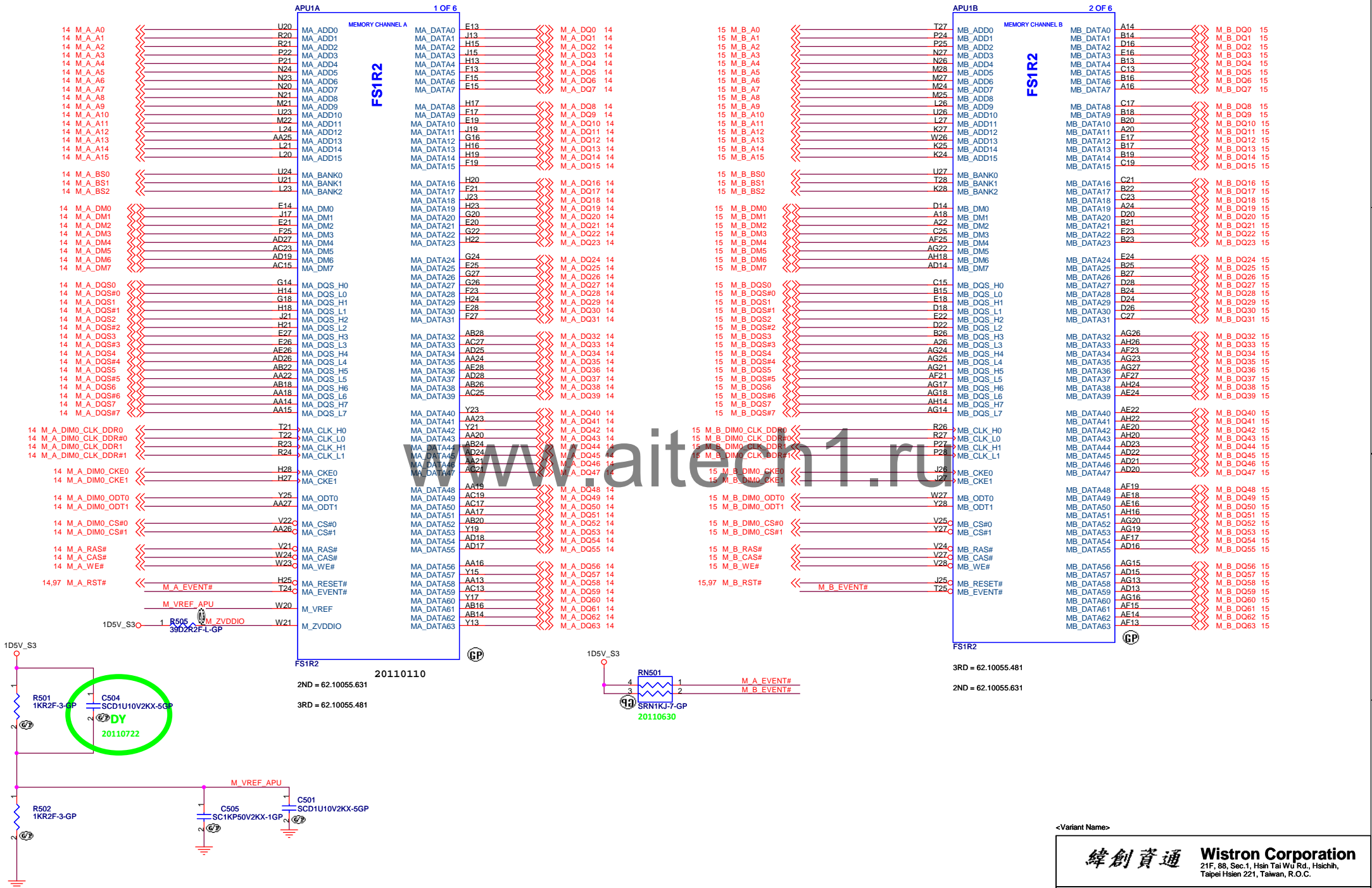
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Table of Content	
Size A3	Document Number S series Popeye & Pebble
Date: Monday, March 12, 2012	Rev SA
Sheet 3	of 103

20110713 change to 16 lanes



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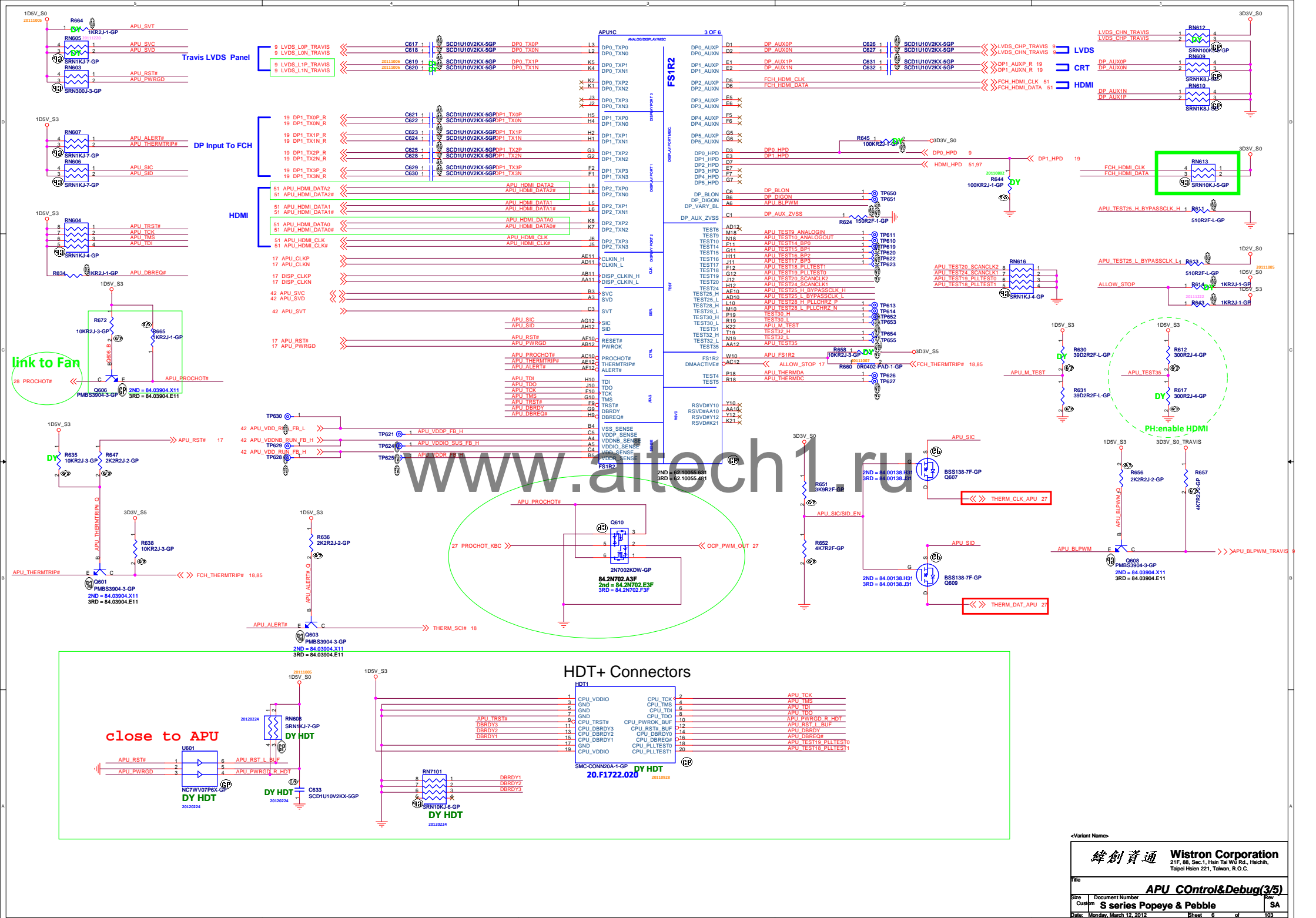
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
APU PCIE(1/5)	
Size A3 Date: Monday, March 12, 2012	Document Number S series Popeye & Pebble Sheet 4 of 103
Rev SB	103

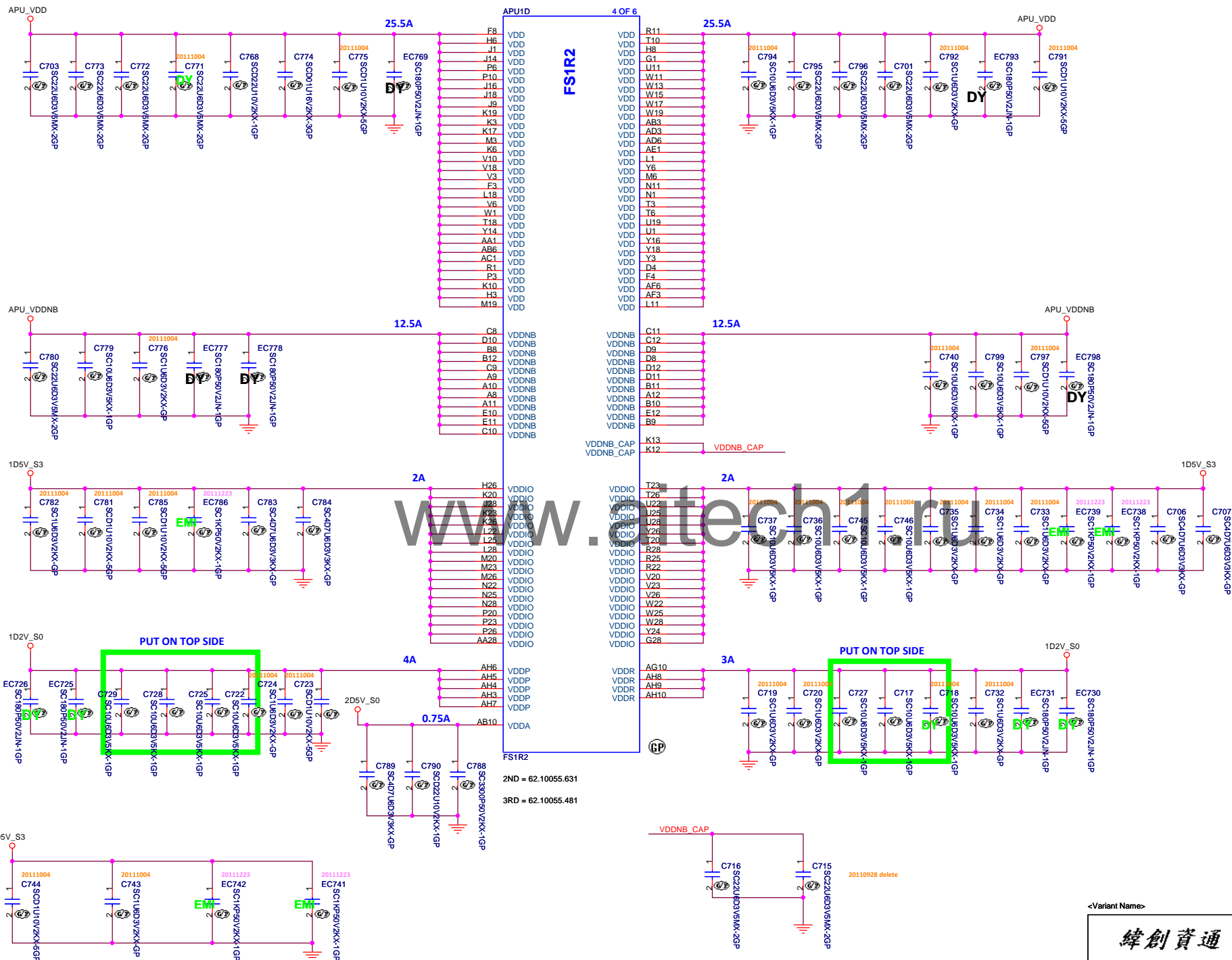


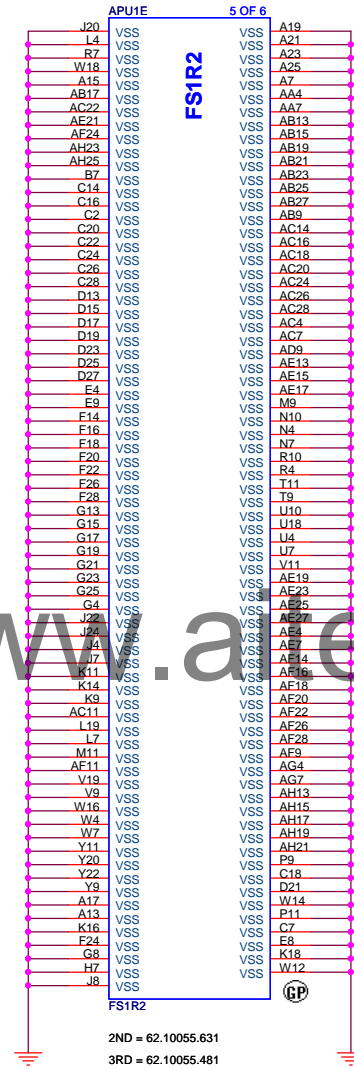
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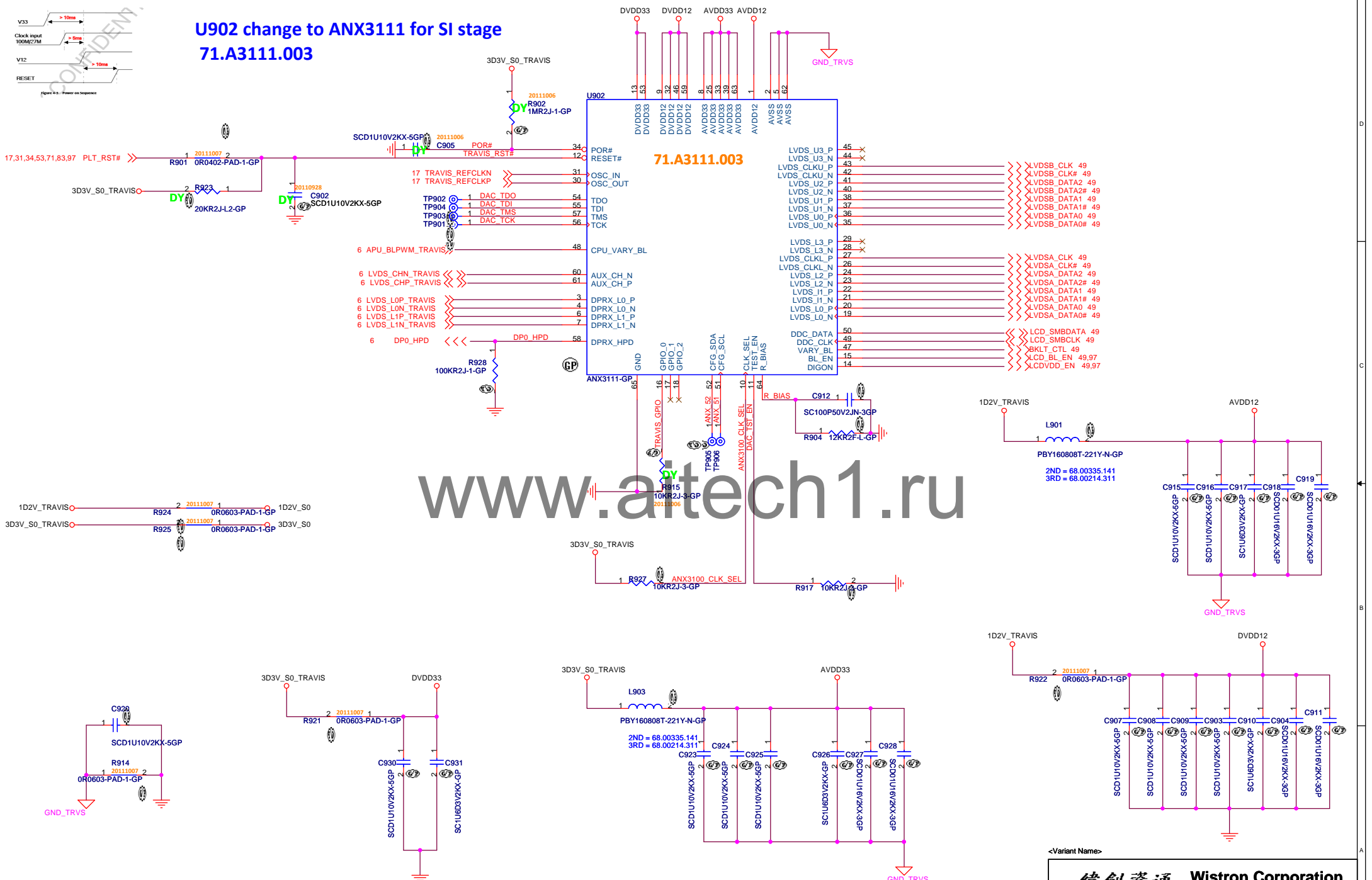
Title			APU DDR(2/5)		
Size	Document Number		S series Popeye & Pebble		Rev
A3					SA
Date:	Monday, March 12, 2012	Sheet	5	of	103







U902 change to ANX3111 for SI stage 71.A3111.003



SSID = MEMORY

DIMM3

5	M_A_A0	98	A0	NP1	NP1
5	M_A_A1	97	A1	NP2	NP2
5	M_A_A2	96	A2		
5	M_A_A3	95	A3	RAS#	110
5	M_A_A4	94	A4	WE#	113
5	M_A_A5	93	A5	CAS#	115
5	M_A_A6	92	A6		
5	M_A_A7	91	A7	CS0#	114
5	M_A_A8	90	A8	CS1#	121
5	M_A_A9	89	A9		
5	M_A_A10	88	A10	CKE0	73
5	M_A_A11	87	A11	CKE1	74
5	M_A_A12	86	A12		
5	M_A_A13	85	A13	CK0#	101
5	M_A_A14	84	A14	CK0#	103
5	M_A_A15	83	A15		
5	M_A_BS2	82	A16/BA2	CK1#	102
5	M_A_BS0	81	BA0	CK1#	104
5	M_A_BS1	80	BA1		
5	M_A_DQ0	79	DQ0		
5	M_A_DQ1	78	DQ1		
5	M_A_DQ2	77	DQ2		
5	M_A_DQ3	76	DQ3		
5	M_A_DQ4	75	DQ4		
5	M_A_DQ5	74	DQ5		
5	M_A_DQ6	73	DQ6		
5	M_A_DQ7	72	DQ7		
5	M_A_DQ8	71	DQ8		
5	M_A_DQ9	70	DQ9		
5	M_A_DQ10	69	DQ10		
5	M_A_DQ11	68	DQ11		
5	M_A_DQ12	67	DQ12		
5	M_A_DQ13	66	DQ13		
5	M_A_DQ14	65	DQ14		
5	M_A_DQ15	64	DQ15		
5	M_A_DQ16	63	DQ16		
5	M_A_DQ17	62	DQ17		
5	M_A_DQ18	61	DQ18		
5	M_A_DQ19	60	DQ19		
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5	M_A_DQS1#	14	DQS1#		
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5	M_A_DQS5#	10	DQS5#		
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5	M_A_DQS7#	8	DQS7#		
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5	M_A_DQS1	6	DQS1		
5	M_A_DQS2	5	DQS2		
5	M_A_DQS3	4	DQS3		
5	M_A_DQS4	3	DQS4		
5	M_A_DQS5	2	DQS5		
5	M_A_DQS6	1	DQS6		
5	M_A_DQS7	0	DQS7		
5	M_A_DIM0_ODT0	116	ODT0		
5	M_A_DIM0_ODT1	117	ODT1		
5	DDR_VREF_CA_S3	126	VREF_CA		
5	DDR_VREF_DQ_S3	127	VREF_DQ		
5	M_A_RST#	30	RESET#		
5	0D75V_S0	203	VTT1		
5		204	VTT2		

DIMM3

NP1	NP1
NP2	NP2
RAS#	M_A_RAS# 5
WE#	M_A_WE# 5
CAS#	M_A_CAS# 5
CS0#	M_A_DIM0_CS#0 5
CS1#	M_A_DIM0_CS#1 5
CKE0	M_A_DIM0_CKE0 5
CKE1	M_A_DIM0_CKE1 5
CK0#	M_A_DIM0_CLK_DDR0 5
CK0#	M_A_DIM0_CLK_DDR0 5
CK1#	M_A_DIM0_CLK_DDR1 5
CK1#	M_A_DIM0_CLK_DDR1 5
DM0	M_A_DM0 5
DM1	M_A_DM1 5
DM2	M_A_DM2 5
DM3	M_A_DM3 5
DM4	M_A_DM4 5
DM5	M_A_DM5 5
DM6	M_A_DM6 5
DM7	M_A_DM7 5
SDA	FCH_SMB0_DATA 15,18,31,65
SCL	FCH_SMB0_CLK 15,18,31,65
EVENT#	198 M_A_EVENT# R 1
VDDSPD	199
SA0	197
SA1	201
NC#1	77
NC#2	122
NC#TEST	125
VDD1	75
VDD2	76
VDD3	81
VDD4	82
VDD5	87
VDD6	88
VDD7	93
VDD8	94
VDD9	99
VDD10	100
VDD11	105
VDD12	106
VDD13	111
VDD14	112
VDD15	117
VDD16	118
VDD17	123
VDD18	124
VSS	13
VSS	14
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VSS	198
VSS	199
VSS	200
VSS	201
VSS	202
VSS	203
VSS	204

DDR3-204P-124-GP

62.10024.D11

2ND = 62.10017.U11

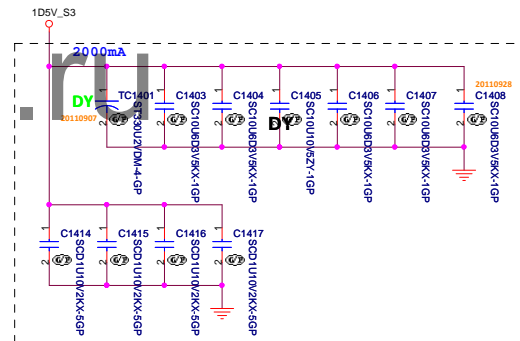
3RD = 62.10024.H71

4TH = 675053-303

20111214

2011007 need use BOM control to
change P/N to 62.10024.J21

Layout note: Place these Caps closed So-Dimm1

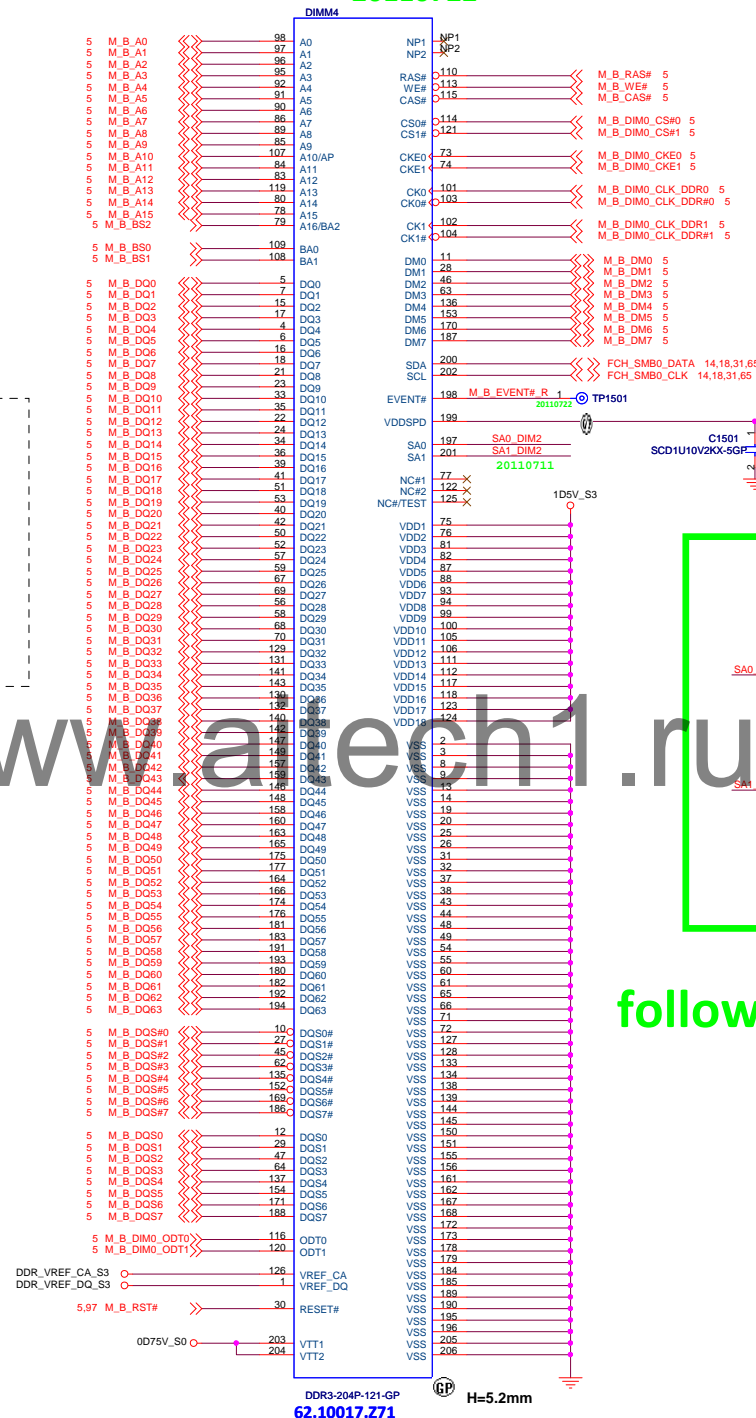
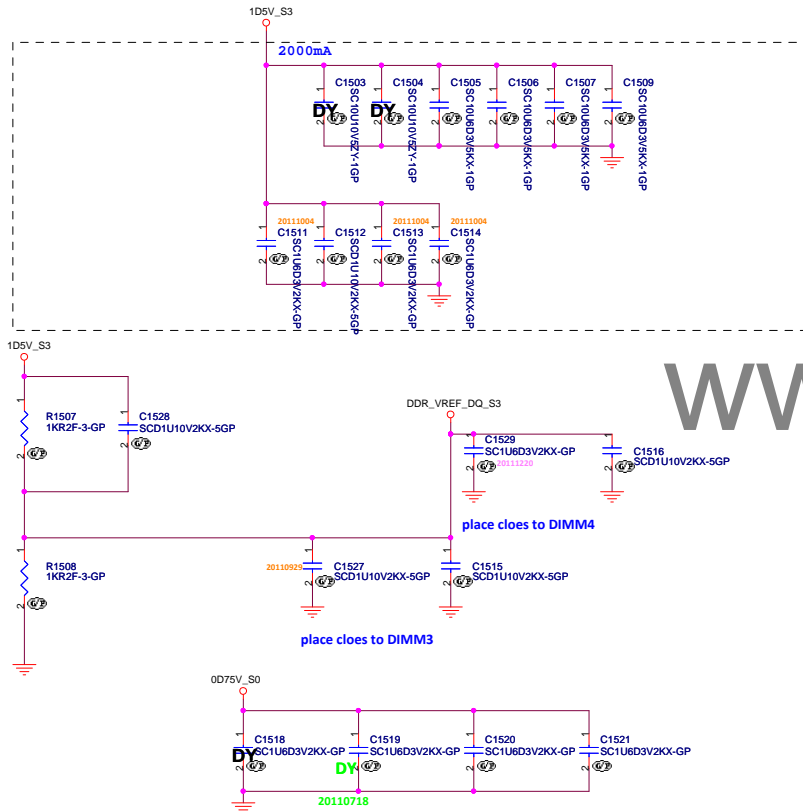


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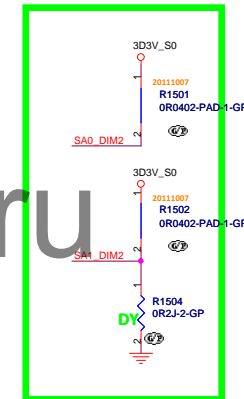
緯創資通 Wistron Corporation		
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Title		
DDR3 SO-DIMM1		
Size	Document Number	Rev
Custom	S series Popeye & Pebble	SA
Date:	Monday, March 12, 2012	Sheet 14 of 103

20110722

Layout note: Place these Caps closed So-Dimm1



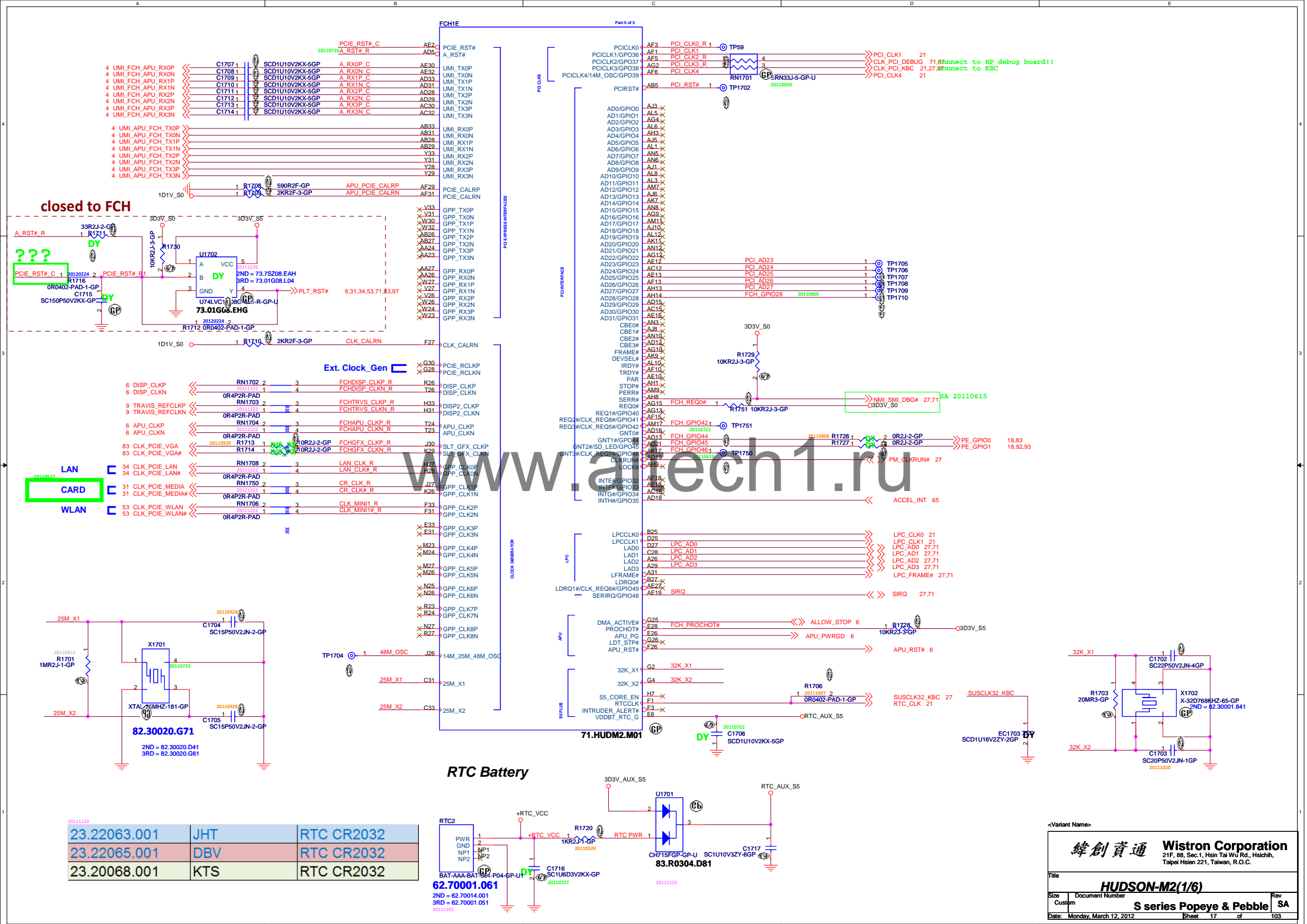
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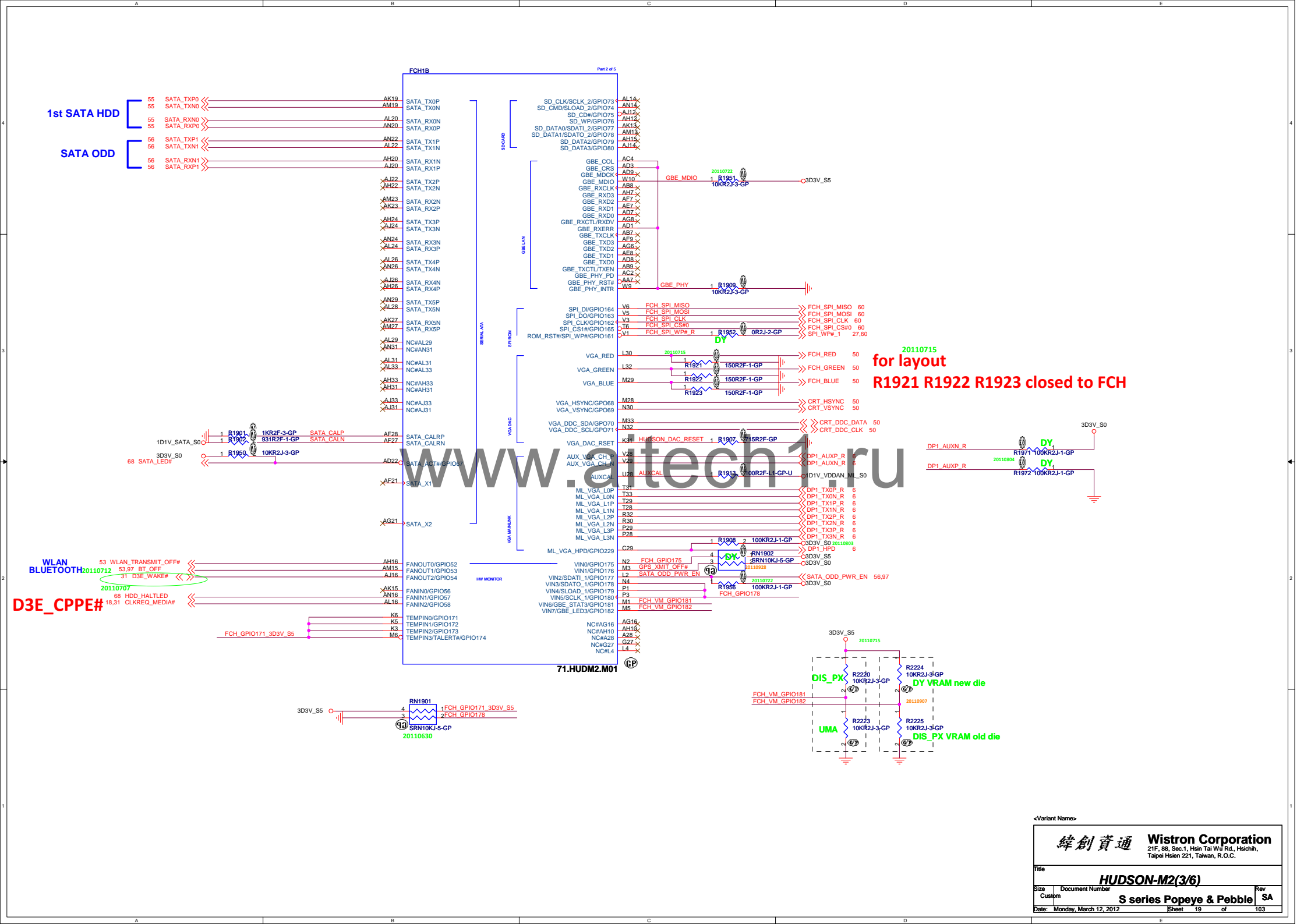


<Variant Name>

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Size	Document Number		Rev
Custom		S series Popeye & Pebble	SA
Date:	Monday, March 12, 2012	Sheet 15 of	103



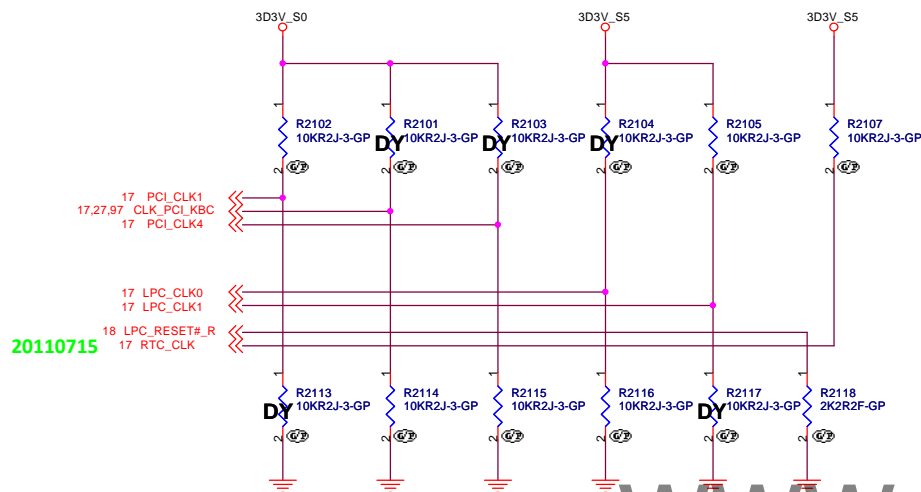


012 Sheet 20 of 103

SSID = S.B

REQUIRED STRAPS

20110707



REQUIRED SYSTEM STRAPS

	LPC_RESET# PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_KBC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

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<Variant Name>

緯創資通

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Title

HUDSON-M2(5/6)

Size
A3

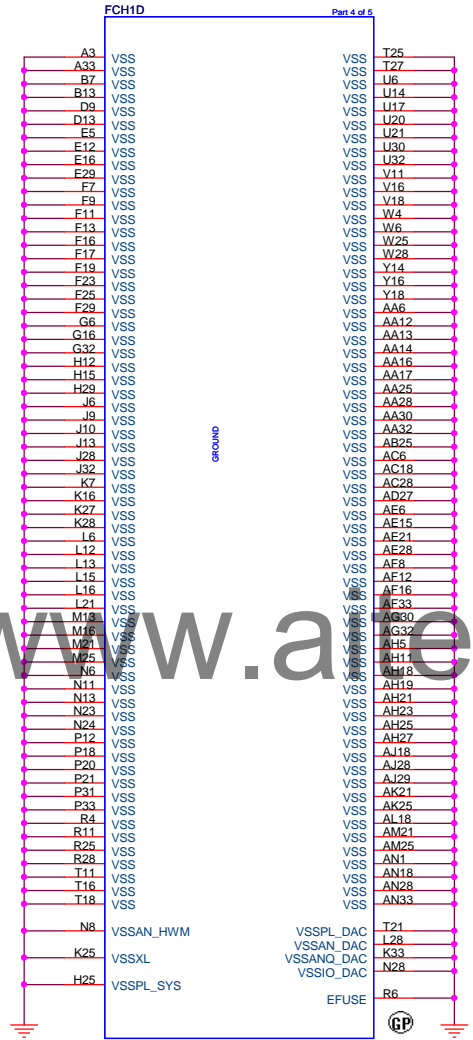
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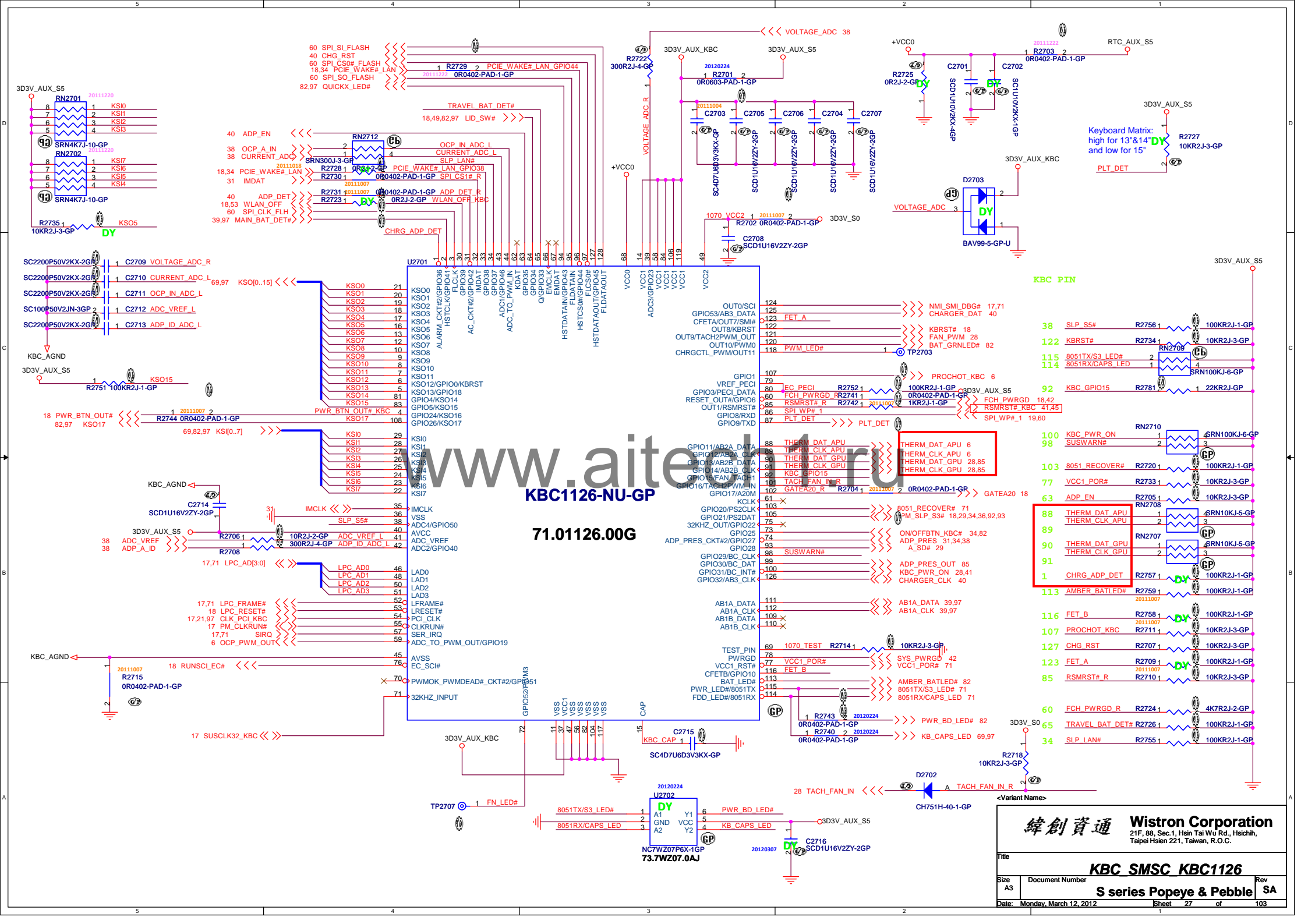
S series Popeye & Pebble

Rev
SA

Date: Monday, March 12, 2012

Sheet 21 of 103





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Title			
KBC SMSC KBC1126			
Size	Document Number		Rev
A3		S series Popeye & Pebble	SA
Date:	Monday, March 12, 2012	Sheet 27 of	103

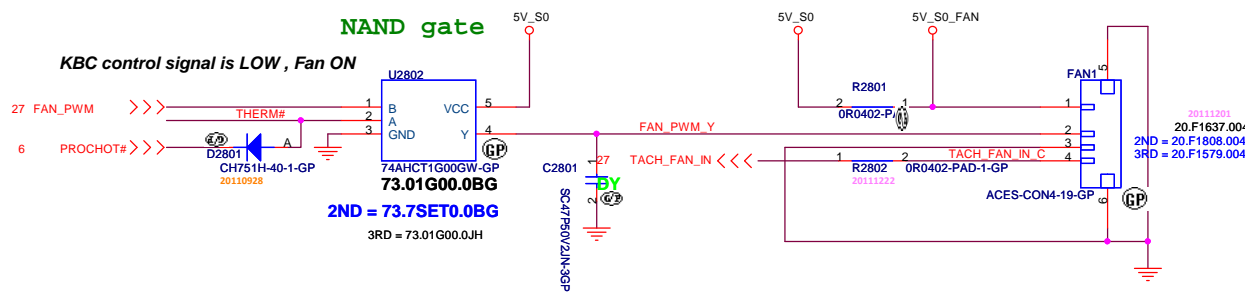
4 WIRE PWM Fan Control circuit

FAN PWM LEVEL = 5V

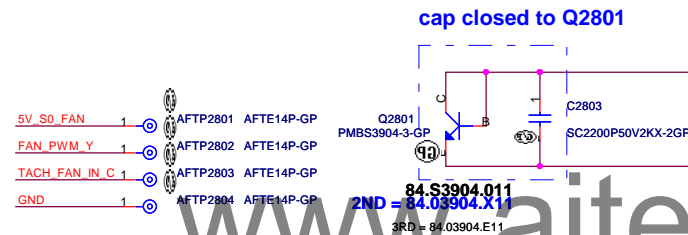
20mil

NAND gate

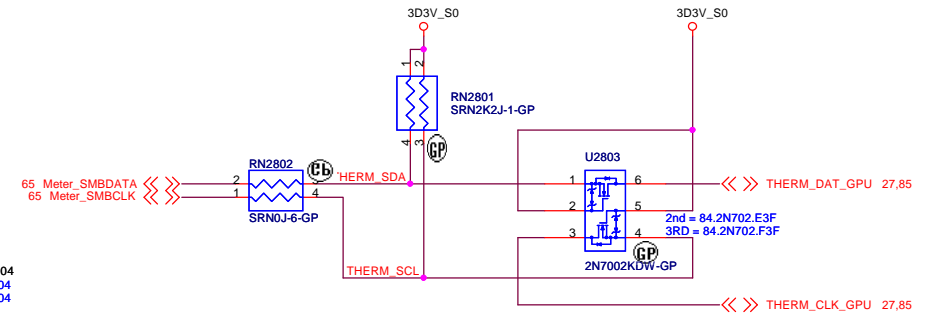
KBC control signal is LOW, Fan ON



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

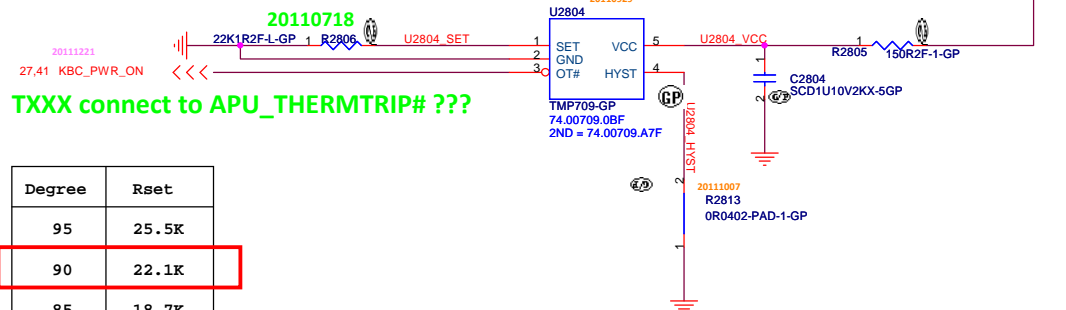


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

90 ° C



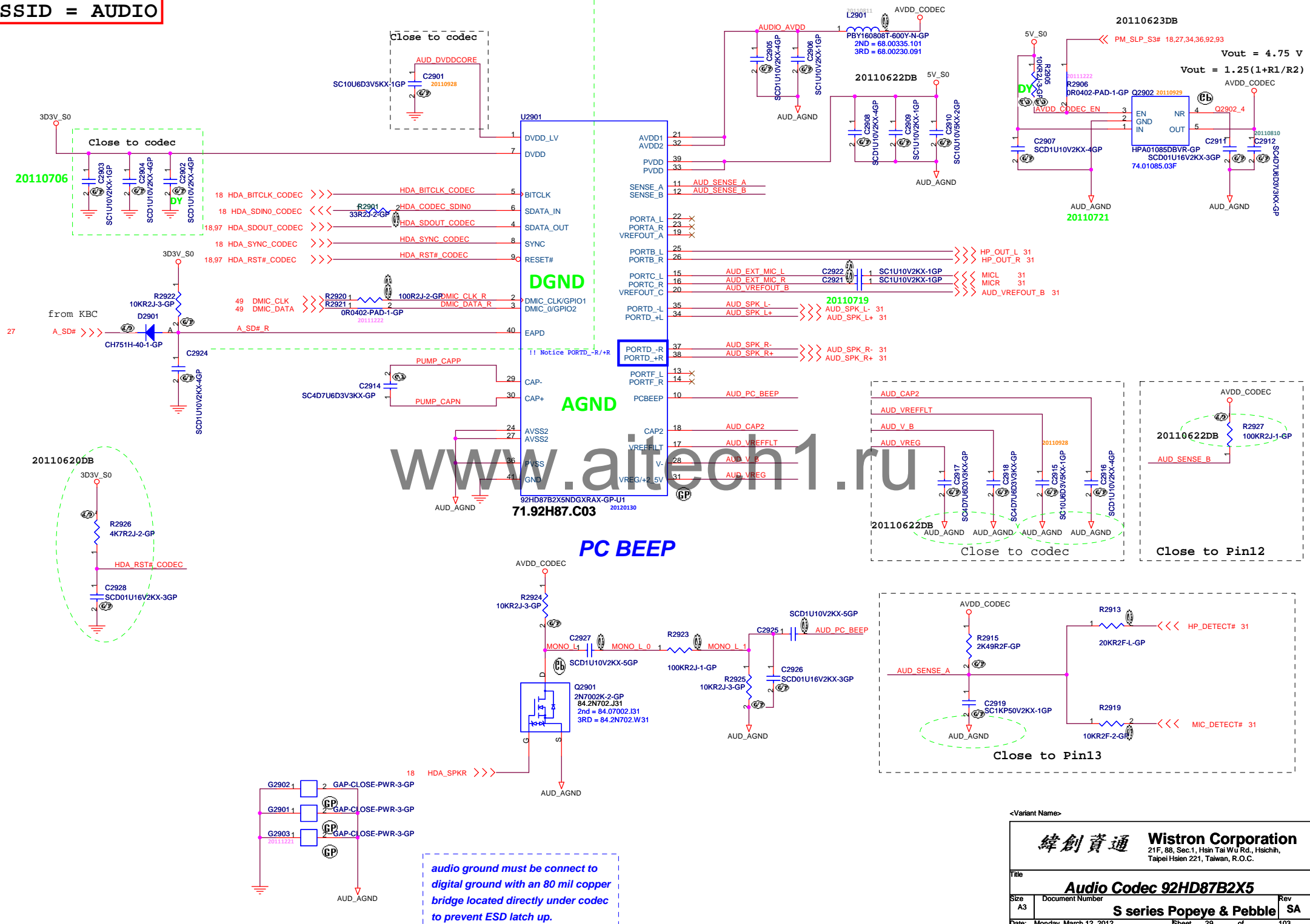
Degree	Rset
95	25.5K
90	22.1K
85	18.7K

<Variant Name>

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Title			
Thermal G781 / FAN			
Size	Document Number	Rev	SA
A3	S series Popeye & Pebble	SA	
Date:	Monday, March 12, 2012	Sheet 28	of 103

SSID = AUDIO



0622-2 SA Change to ADUIO BOARD page3

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<Variant Name>			
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
External MIC Pre-Amp			
Size	Document Number	Rev	
A3	S series Popeye & Pebble	SA	
Date:	Monday, March 12, 2012	Sheet	30 of 103

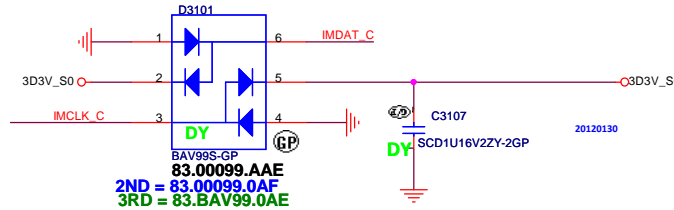
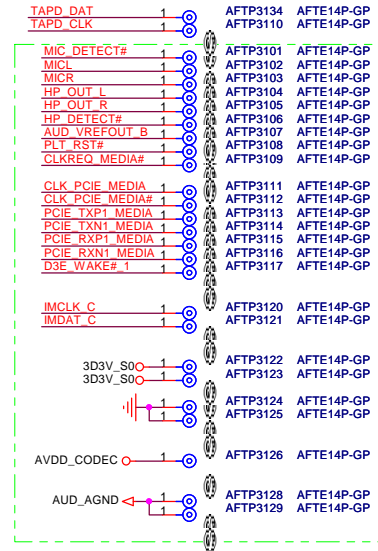
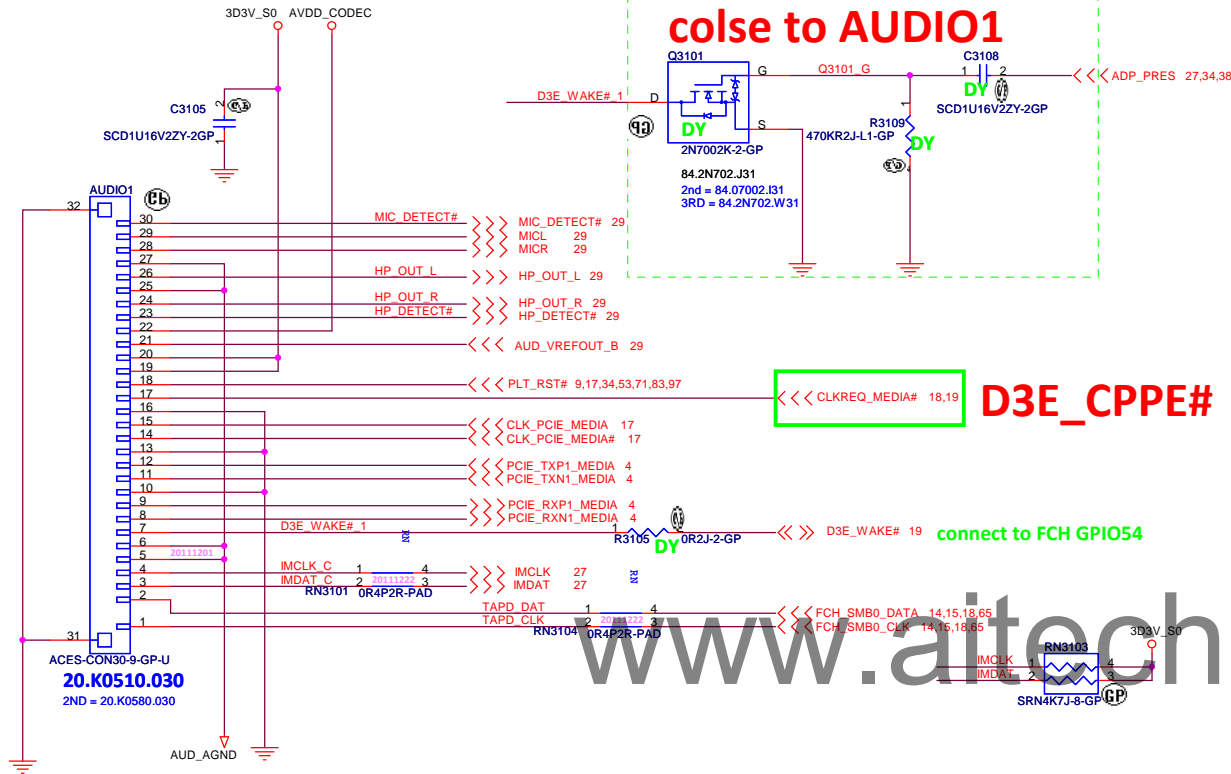
Audio Board +Touch Pad Connector

HeadPhone OUT

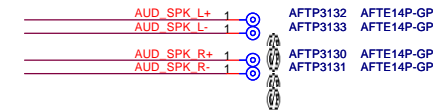
0621 SA Change to ADUIO BOARD page4

Jack Detect

0621 SA Change to ADUIO BOARD page4



Speaker Connector



<Variant Name>

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Title				
AUDIO Connector				
Size	Document Number			Rev
A3	S series Popeye & Pebble			SA
Date:	Monday, March 12, 2012	Sheet	31 of	103

CardReader JMicron JMB709

0622-2 SA Change to ADUIO BOARD page1

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0622-2 SA Change to ADUIO BOARD page2

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20110624 DY

3D3V_LAN_S5

LAN_GPO R3406 10K 1KR2J-1-GP

LAN_SMBDATA R3418 10K 10KR2J-3-GP

EEDI R3408 10K 10KR2J-3-GP

EECS R3409 10K 10KR2J-3-GP

3D3V_LAN_S5

40 mils (average 100mA)

R3403 20111007

DR0603-PAD-1-GP

VDDREG

C3424 SCD100/2KX-GSP

C3422 SCD100/2KX-GSP

C3403 SCD100/6/2Z-2SP

C3417 SCD100/2KX-GSP

C3418 SCD100/2KX-GSP

C3414 SCD100/2KX-GSP

C3419 SCD100/2KX-GSP

C3406 SCD100/3KX-GP

Place closed to Pin 34,35

cap near pin12,27,39,42,47,48 <200mils

Put cap near pin21

EVDD10

R3417

C3412

C3409

0R0603-PAD-1-GP

SCD1U06VZXX-2GP

SCD1U06VZXX-2GP

cap near pin3,6,9,13,29,41,45

VDD10

C3423

C3420

C3407

C3421

C3435

C3416

C3415

SCD1U06VZXX-5GP

SCD1U06VZXX-5GP

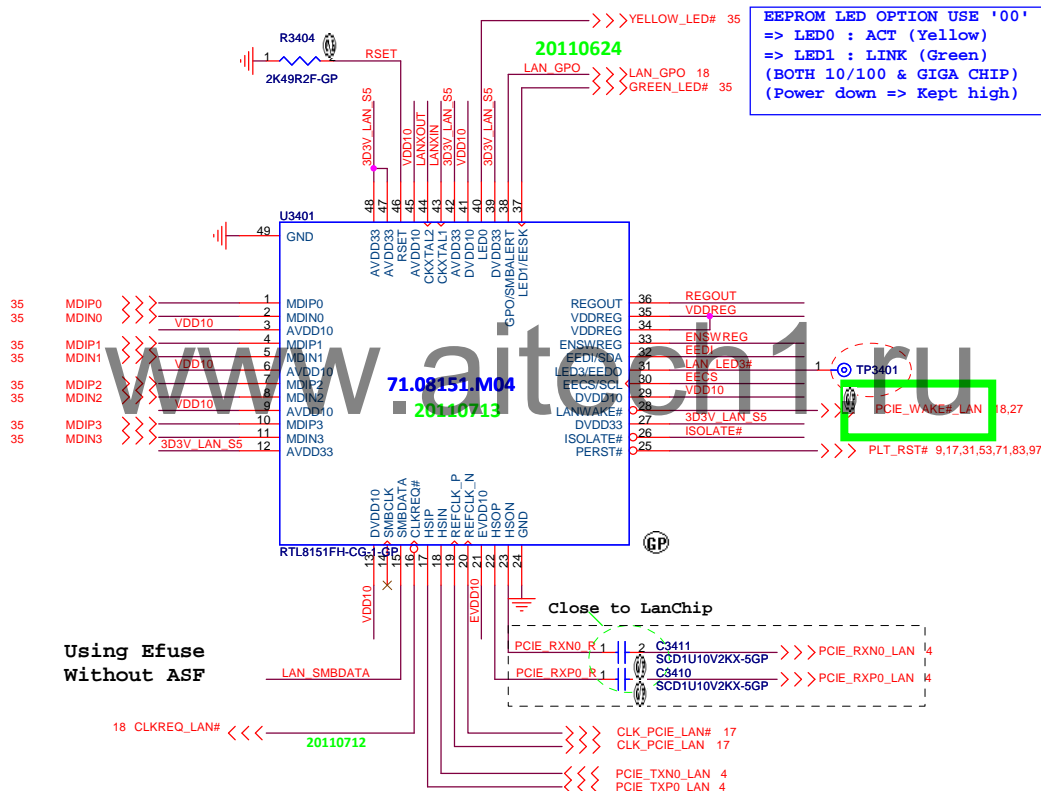
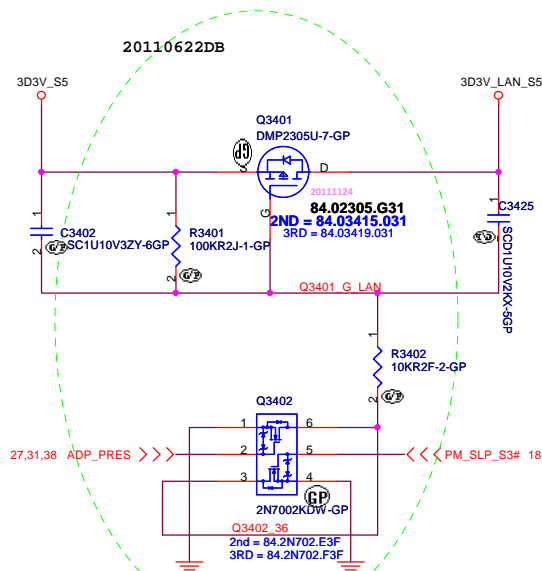
SCD1U06VZXX-5GP

SCD1U06VZXX-2GP

SCD1U06VZXX-2GP

SCD1U06VZXX-5GP

SCD1U06VZXX-5GP

[illegible]

REGOUT

L3401

100µH ±12-6P

201110615DB

C3401

100µF

C3413

100µF

SCD1UN072XK-56P

LAN Power Inductance Spec

- (1) IDC >= 600mA
- (2) Tolerance < 20%
- (3) RDC <= 0.8ohms(Max)
- (4) Efficiency >= 80%

Put 4D7U L + 22U cap near pin36 <200mils
(2nd = 78.22610.81L)

ENSWREG

1 20111007 2

R3405 0R0402-PAD-1-GP

3D3V_LAN_S5

R3407 0R2J-2-GP

PH = Enable

PL = Disable

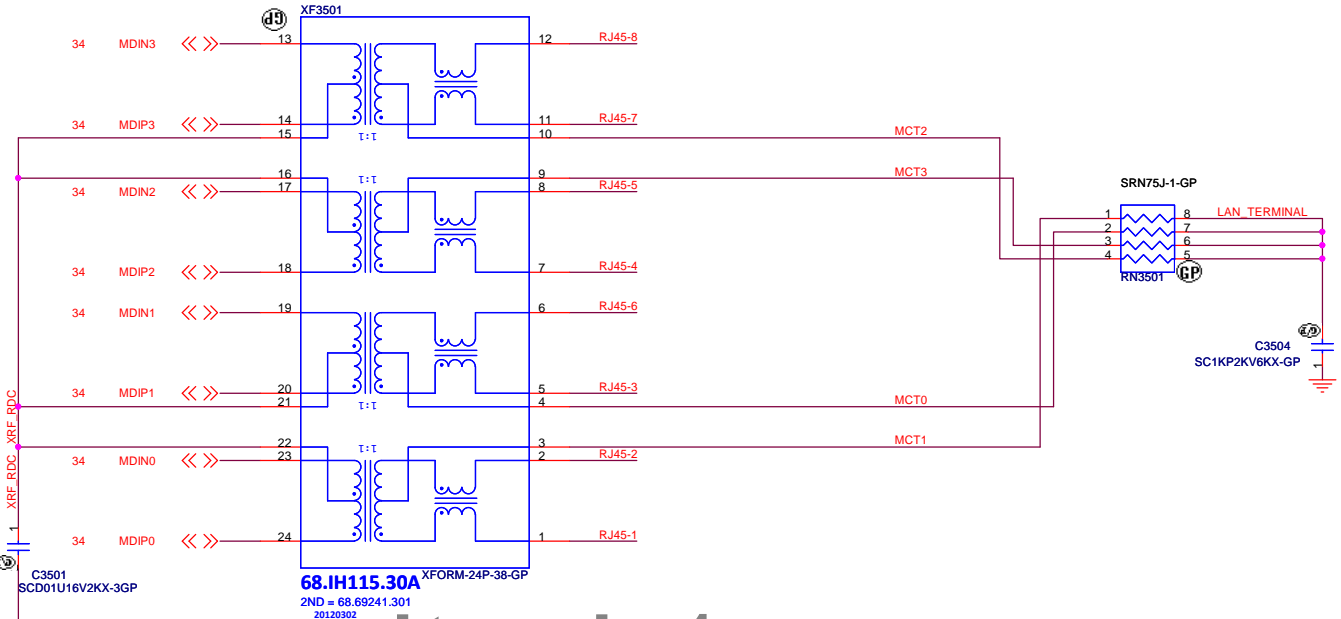
ENSWREG (REGOUT 1D05V)

[illegible]

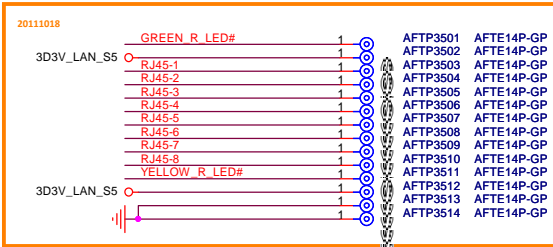
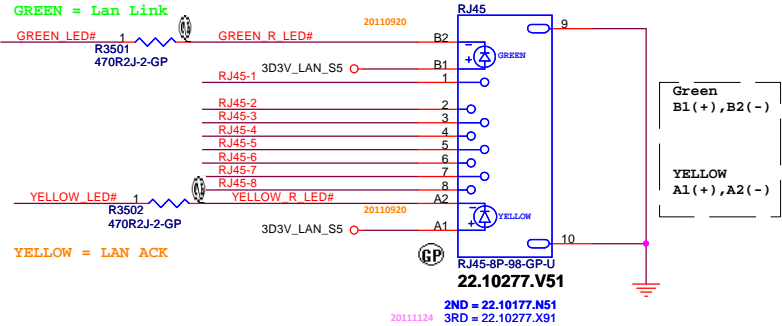
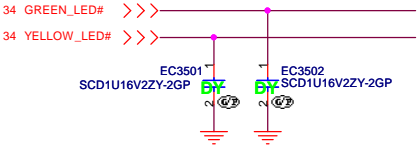
```
KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO      => EFuse Strap Pin
```

White LED for connectivity and Amber LED for activity located on RJ-45 connector

close to XF3501

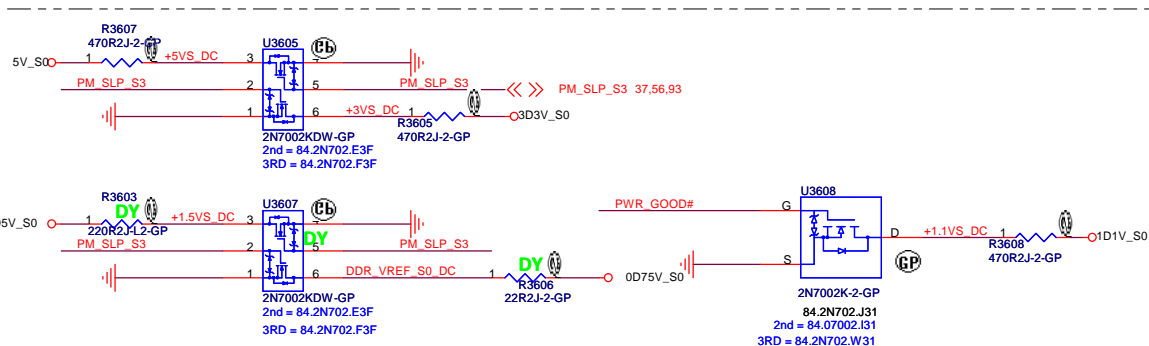
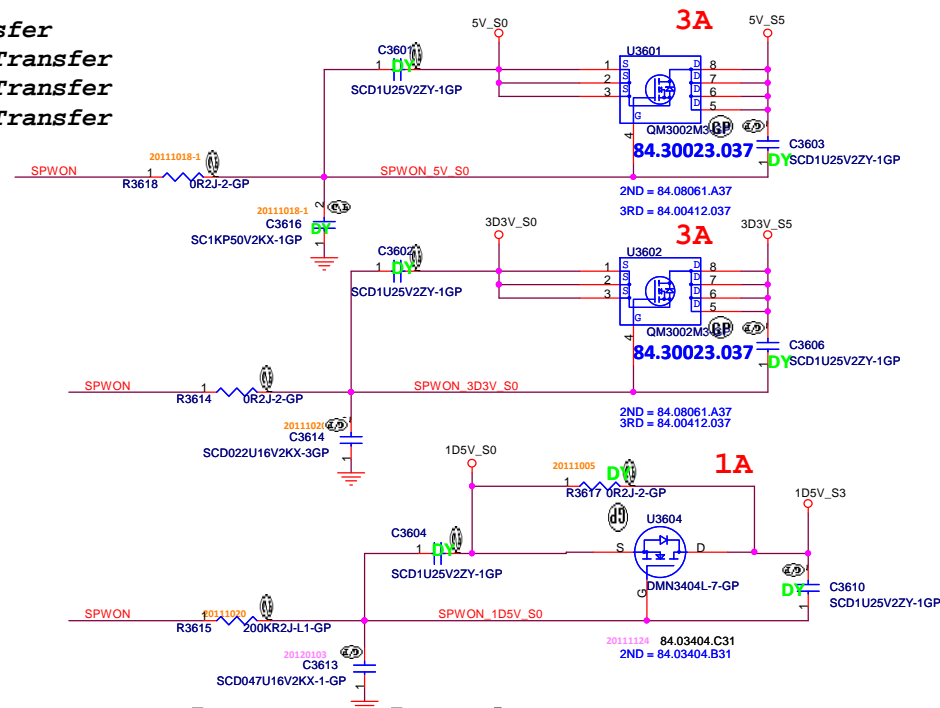


RJ45 Connector



- (1) route on bottom as differential pairs.
- (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- (3) No vias, No 90 degree bends.
- (4) pairs must be equal lengths.
- (5) 6mil trace width, 12mil separation.
- (6) 36mil between pairs and any other trace.
- (7) Must not cross ground moat, except RJ-45 moat.

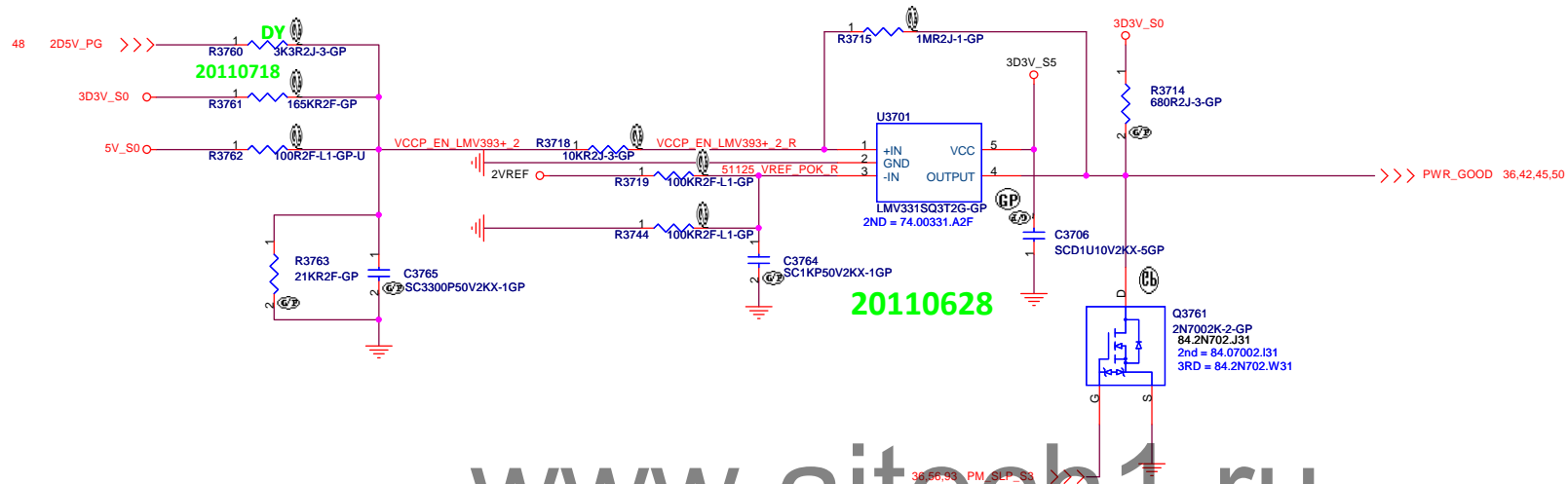
5V_S5 to 5V_S0 Transfer
3D3V_S5 to 3D3V_S0 Transfer
1D5V_S3 to 1D5V_S0 Transfer
1D1V_S5 to 1D1V_S0 Transfer



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Plane Enable			
Size A3	Document Number		Rev
	S series Popeye & Pebble		SA
Date:	Monday, March 12, 2012	Sheet 36 of	103

POK



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<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

POK

Size
A3

Document Number

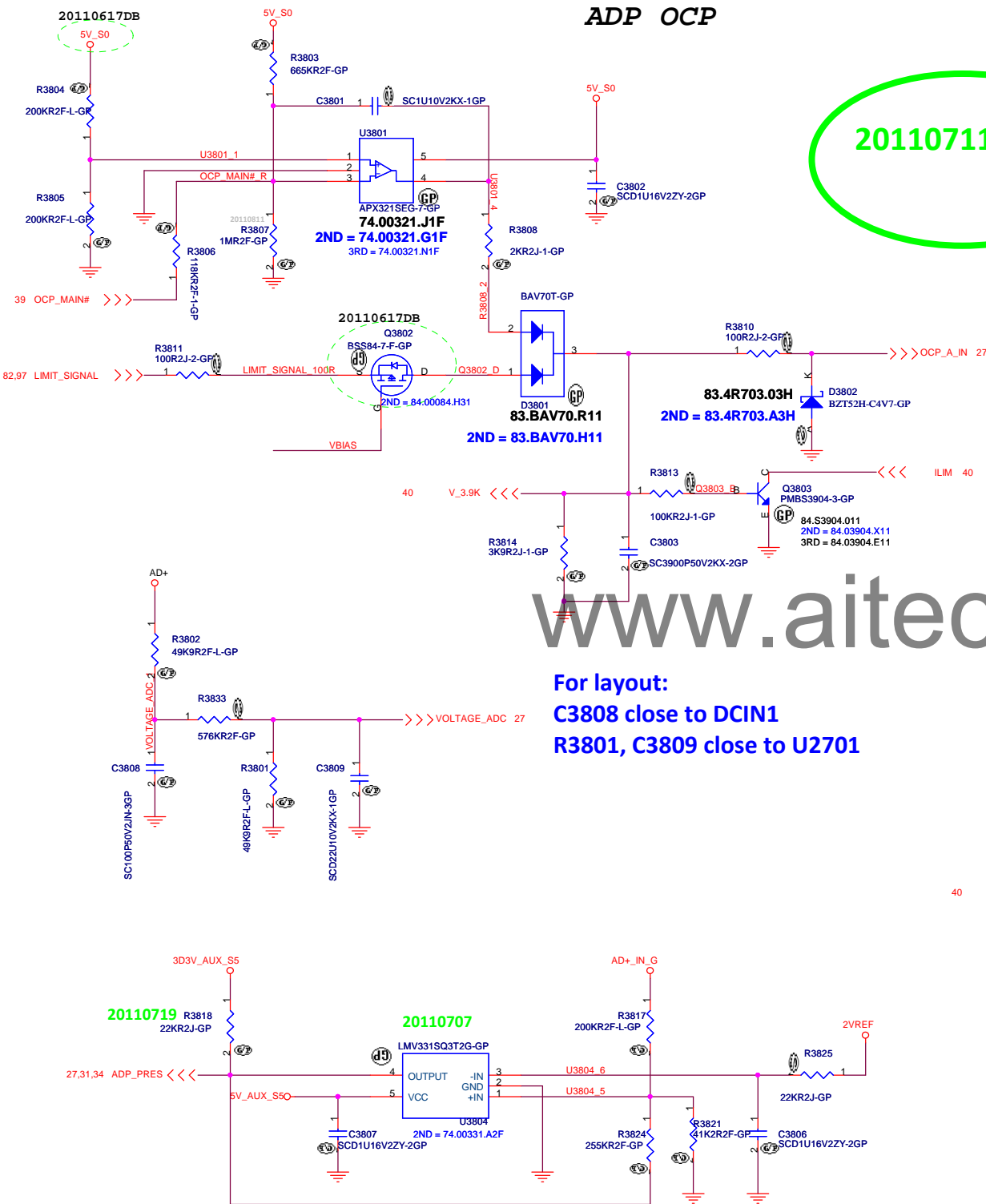
S series Popeye & Pebble SA

Date: Monday, March 12, 2012

Sheet 37 of 103

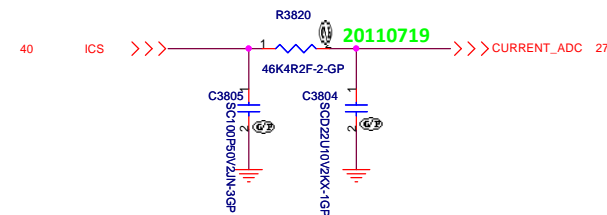
ADP OCP

20110711 delete



www.aitech1.ru

For layout:
C3808 close to DCIN1
R3801, C3809 close to U2701

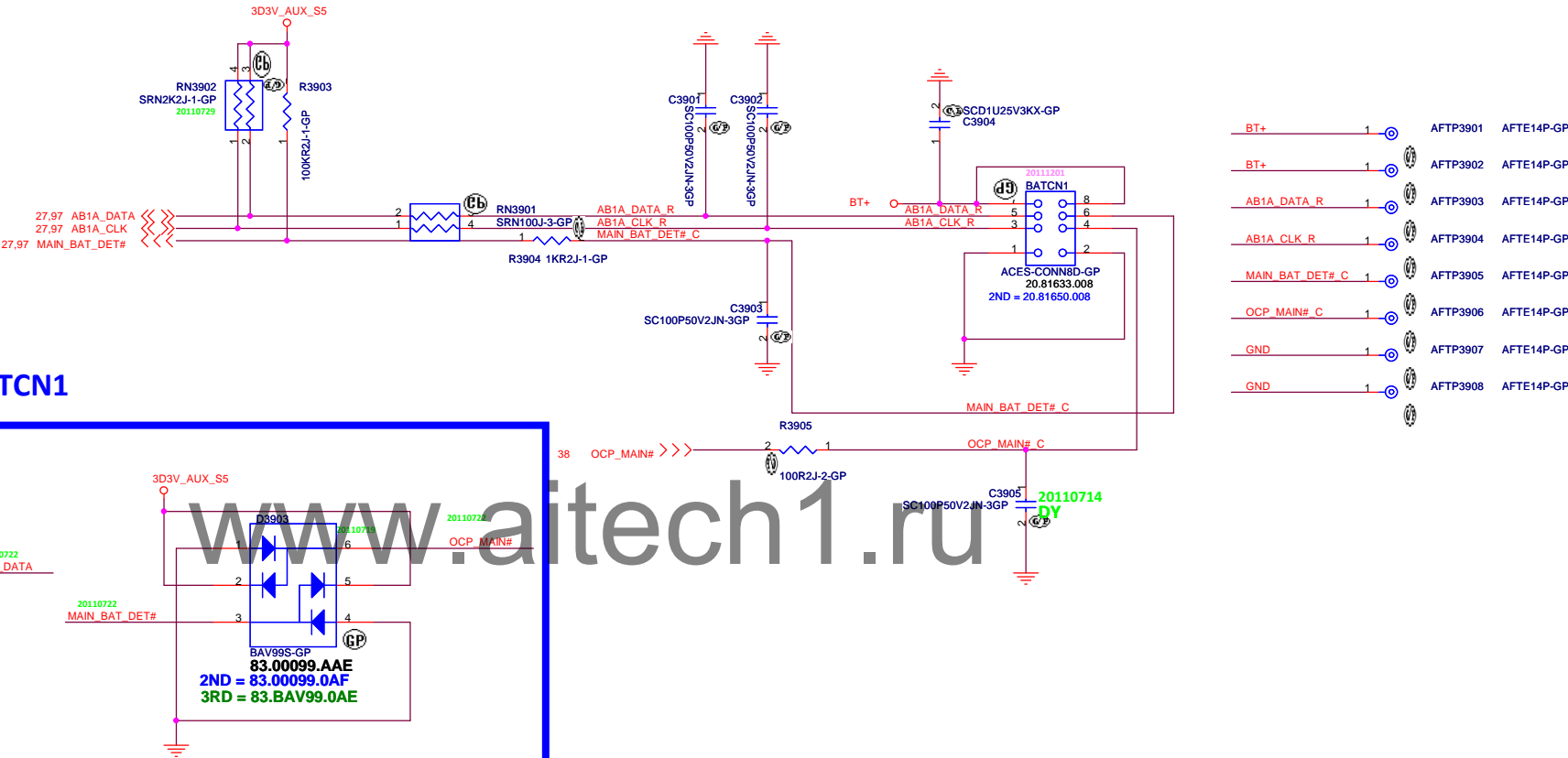


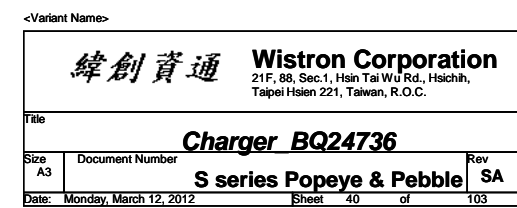
<Variant Name>

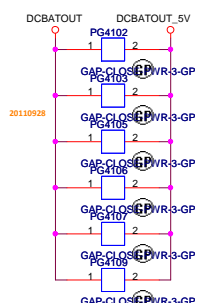
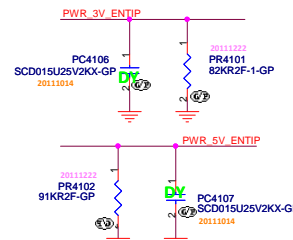
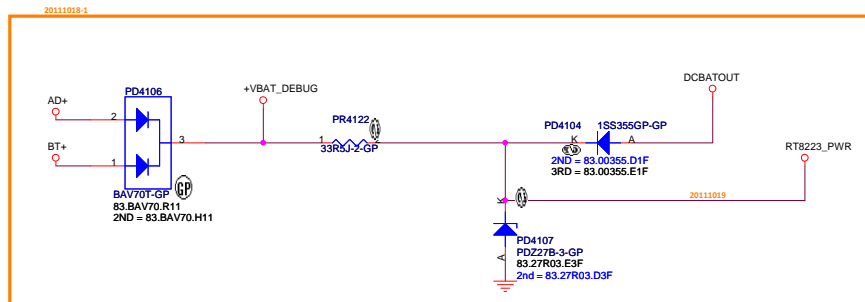
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

ADP OCP			
S series Popeye & Pebble			
Size A3	Document Number	Rev SA	
Date: Monday, March 12, 2012	Sheet 38	of 103	

Battery Connector





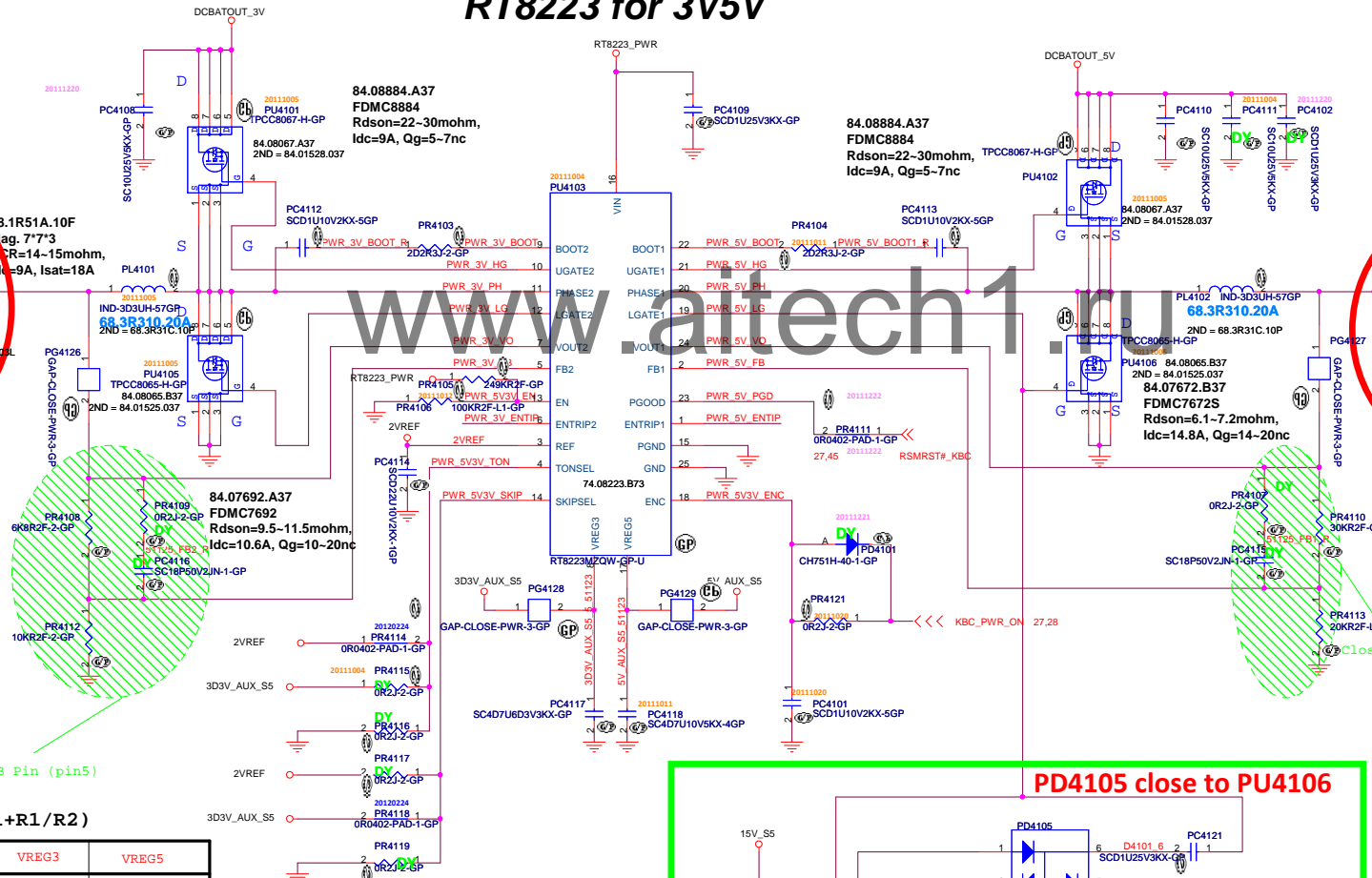


RT8223 for 3V5V

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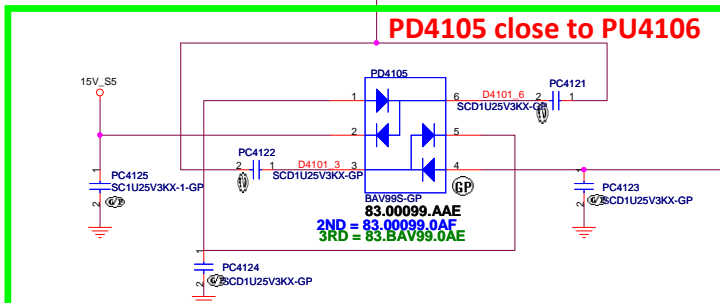
Iomax=5A
OCF setting < 10A

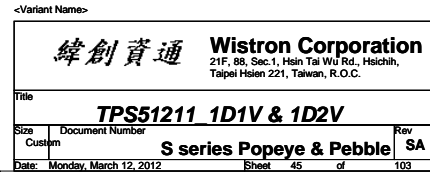
Iomax=6A
OCF setting < 10.5A

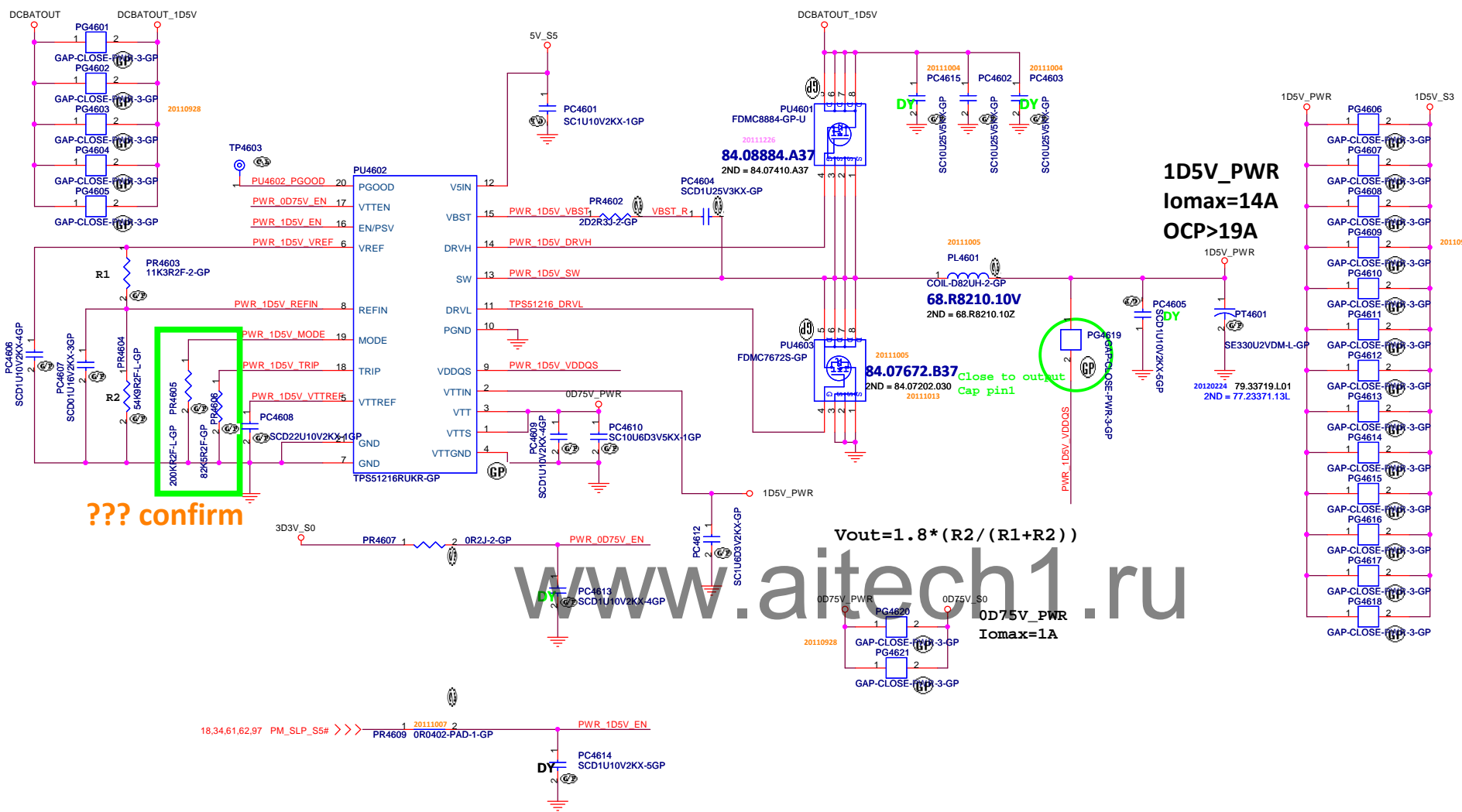


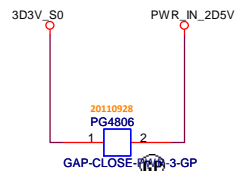
$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

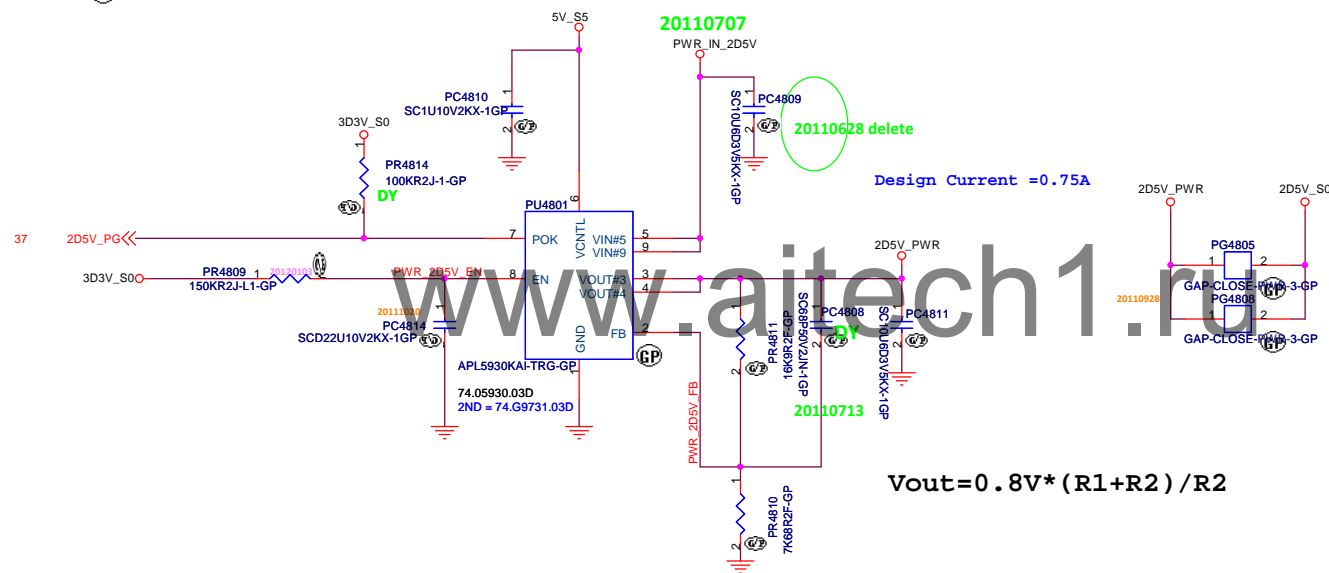


TPS51211 for 1D2V





APL5930 for 2D5V_S0



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

APL5930 2D5V

Size
A3

Document Number

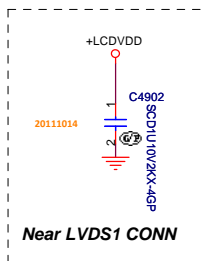
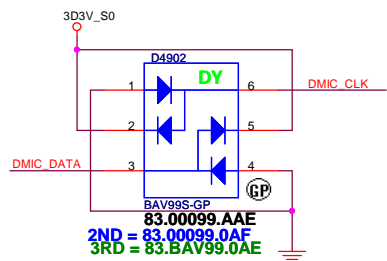
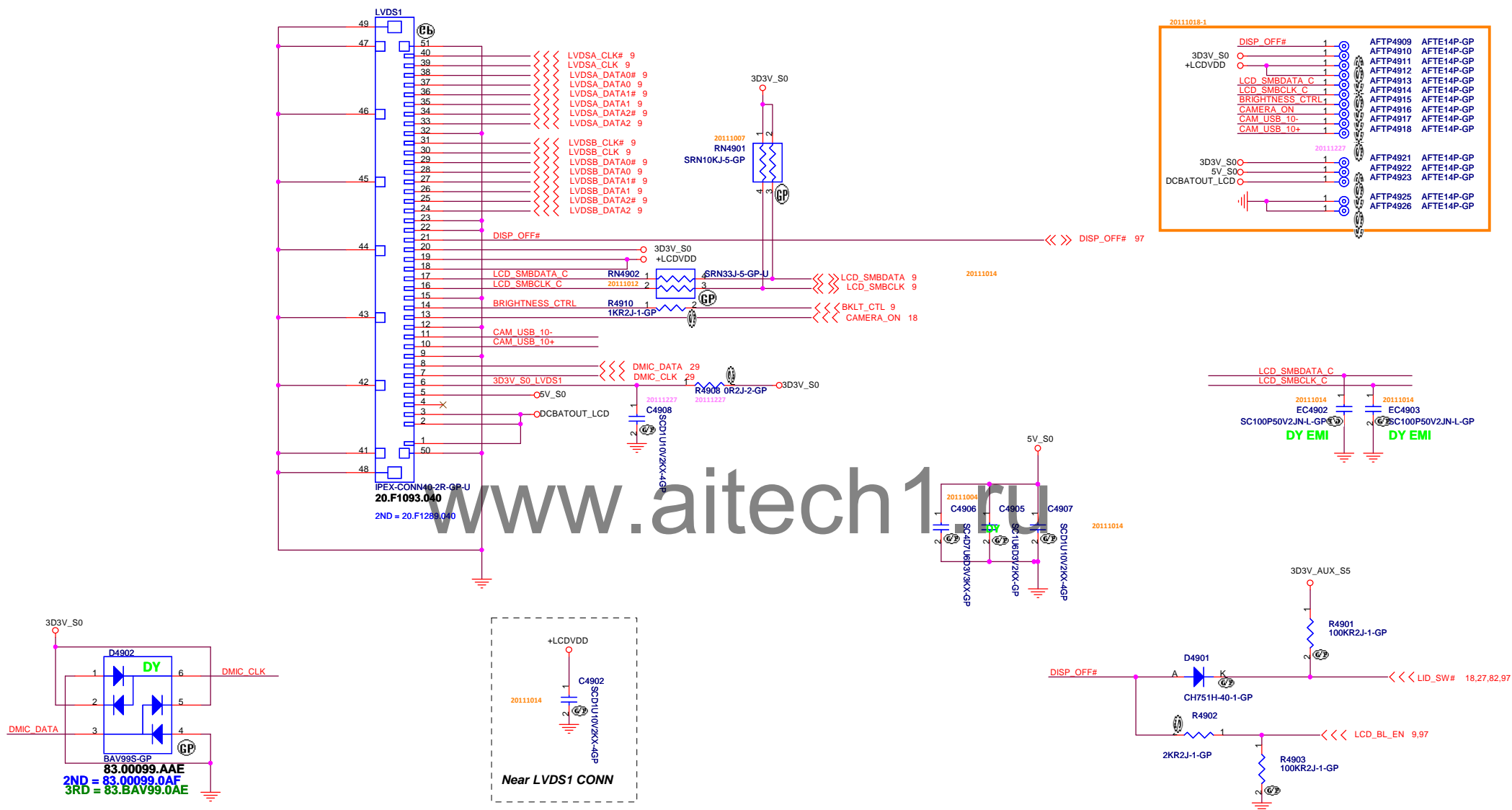
S series Popeye & Pebble

Rev
SA

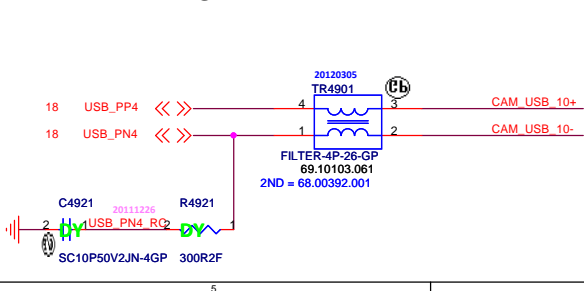
Date: Monday, March 12, 2012

Sheet 48 of 103

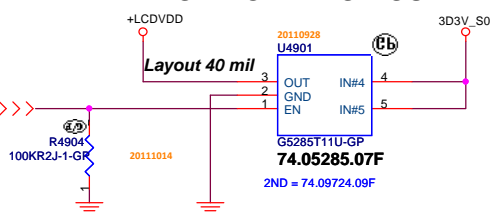
LCD Connector



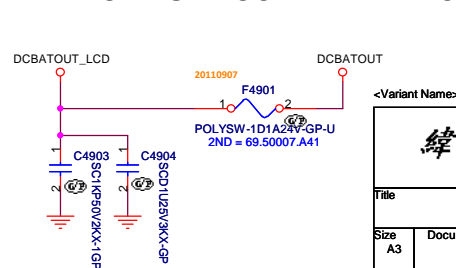
CAMERA



LCD POWER CIRCUIT

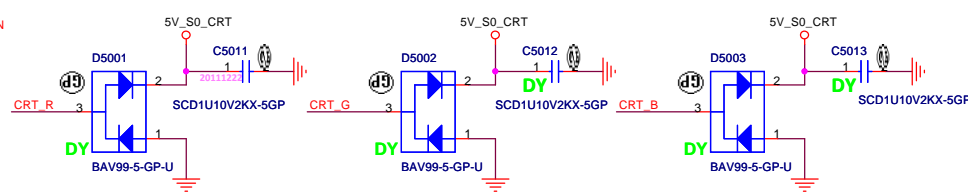
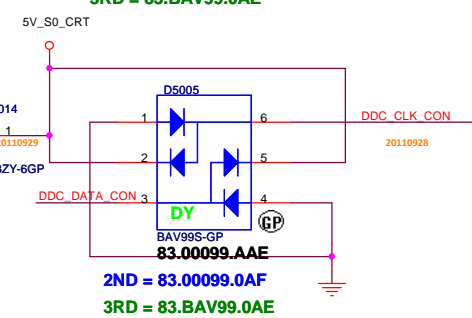
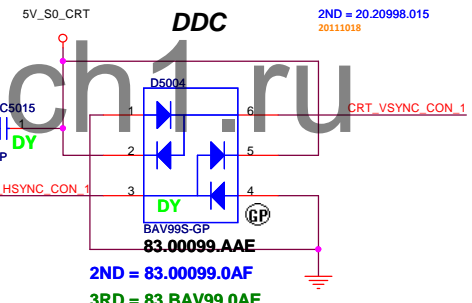
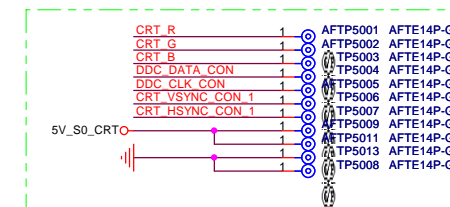


LED BACKLIGHT CONVERTER POWER

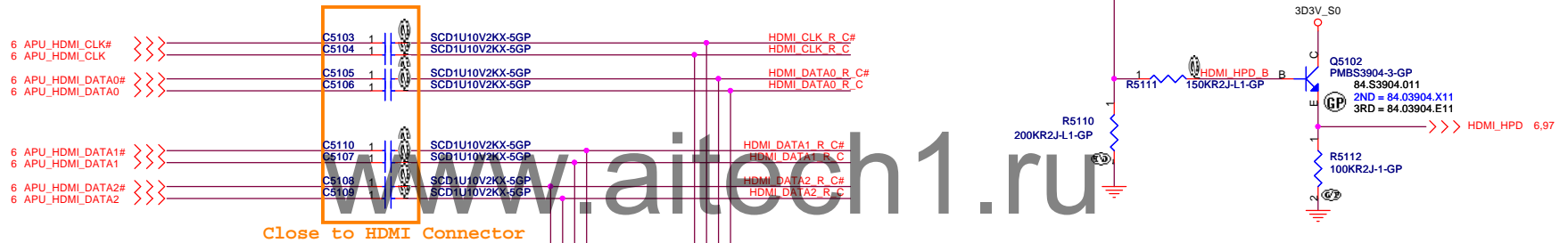
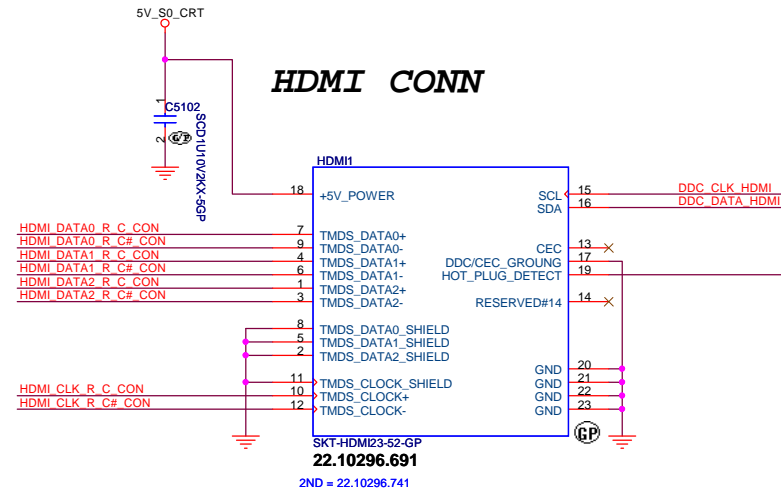
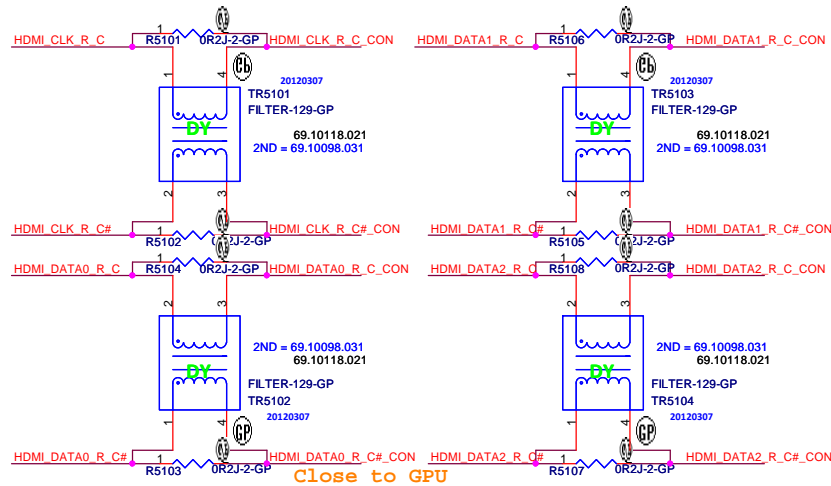


緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

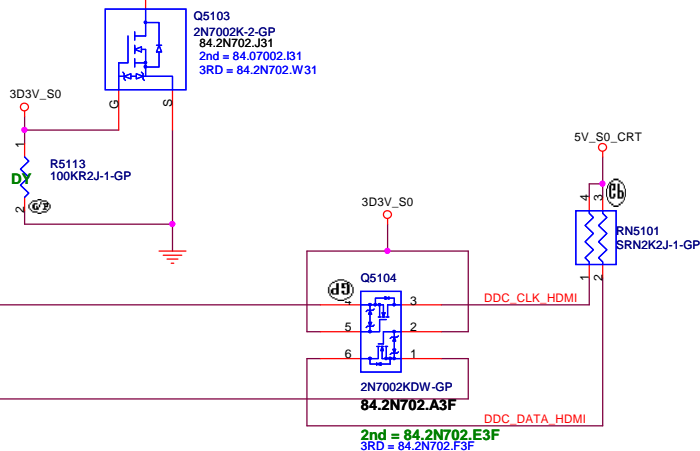
FCH RGB to first R is 37.5 ohm with in 500 mil
First R to second R is 50 ohm
Second R to filter is 75 ohm(>50 ohm) to connector
Final CAP side to connector with 200 mil
ESD part to connector with 300 mil,width is 20mil



HDMI Connector



Close to HDMI Connector



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).

The total delay on CTRLDATA should be longer than CTRLCLK.

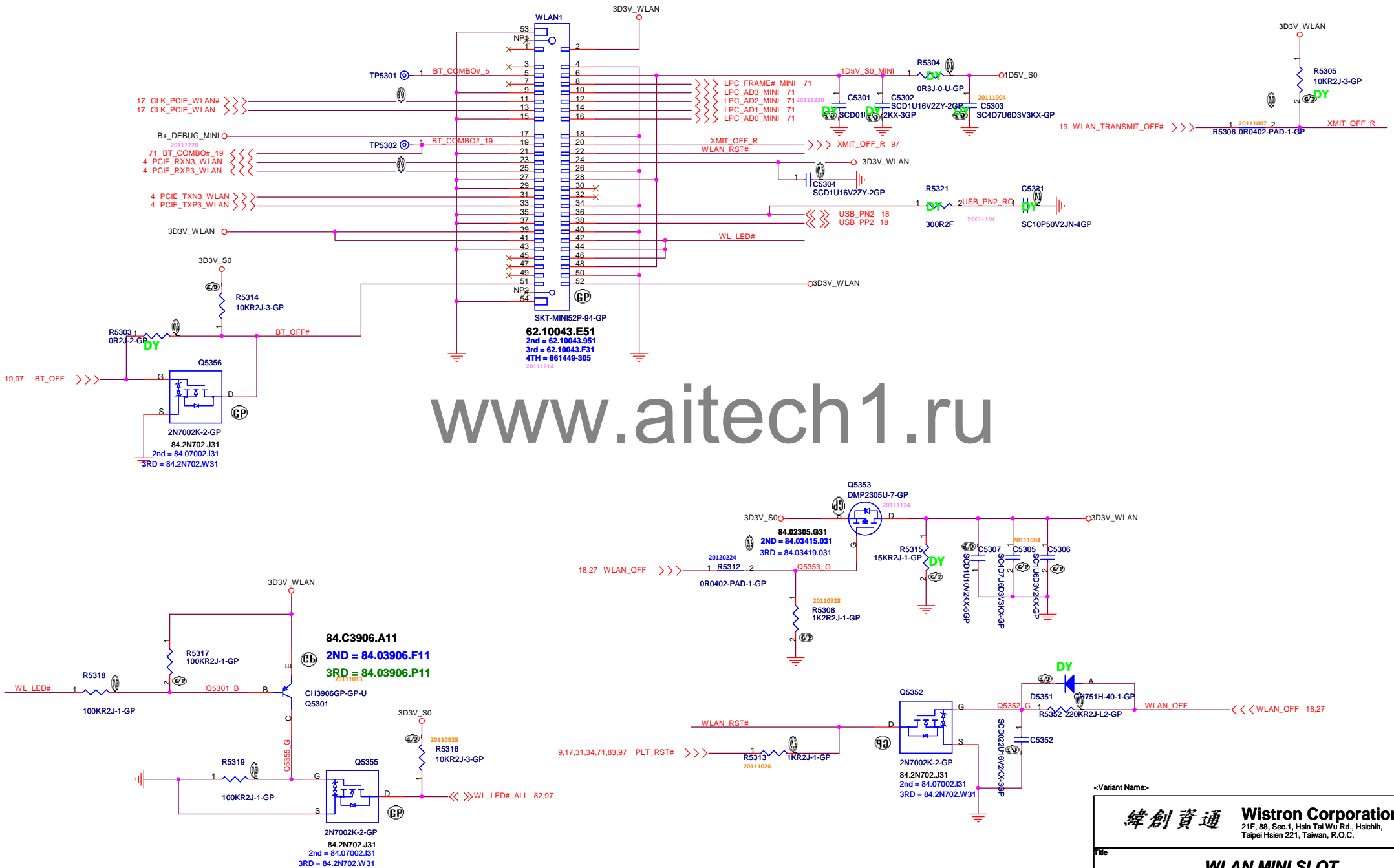
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

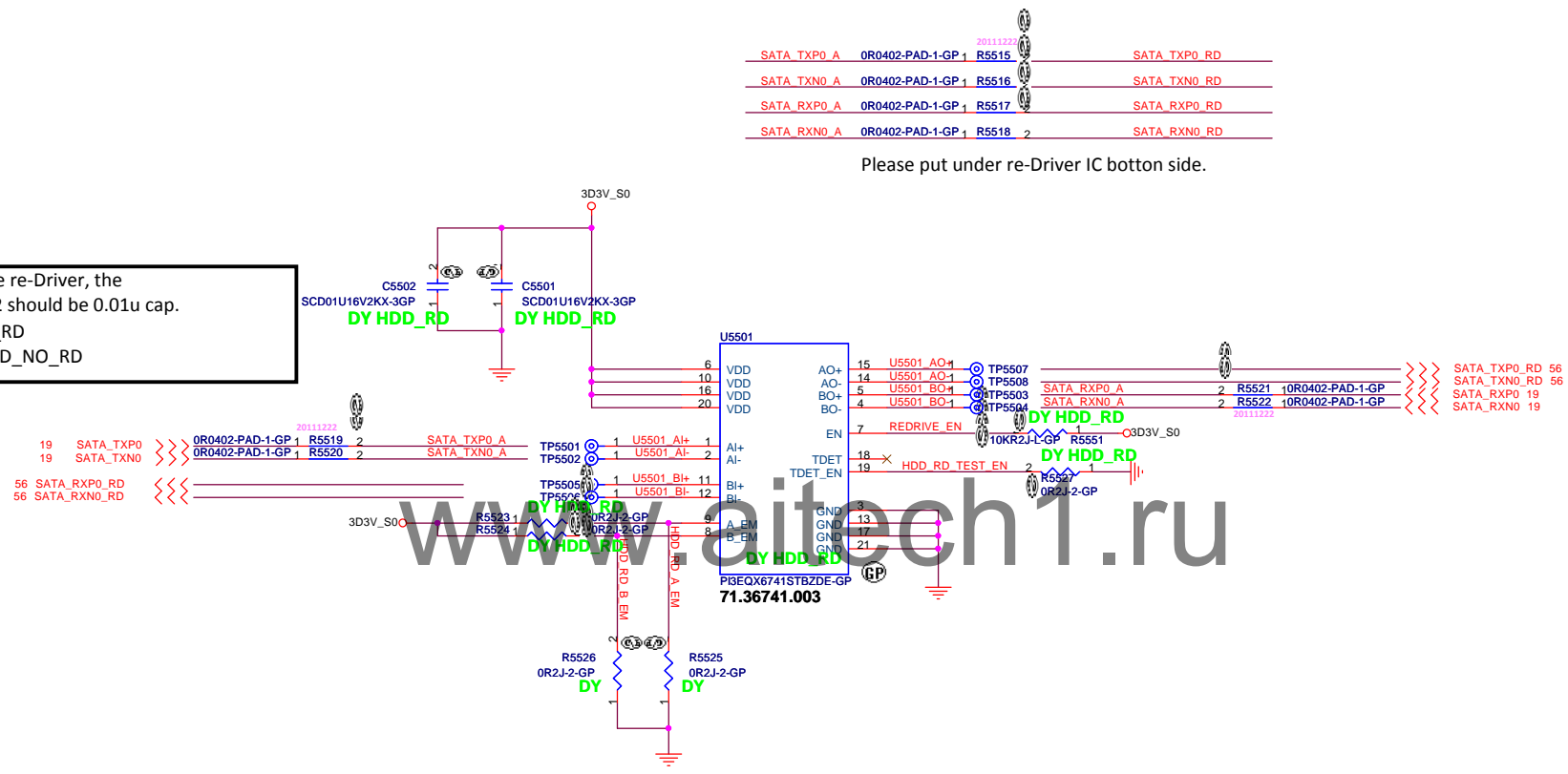
Title		Rev
HDMI Level Shifter/Conn		SA
Size A3	Document Number	S series Popeye & Pebble
Date: Monday, March 12, 2012	Sheet 51	of 103

WLAN Connector

Mini-Card--WLAN (Half)



If we use the re-Driver, the
R5519~5522 should be 0.01u cap.
Install HDD_RD
DUMMY HDD_NO_RD

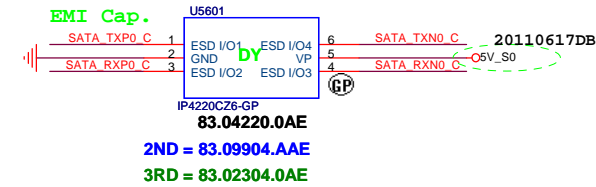
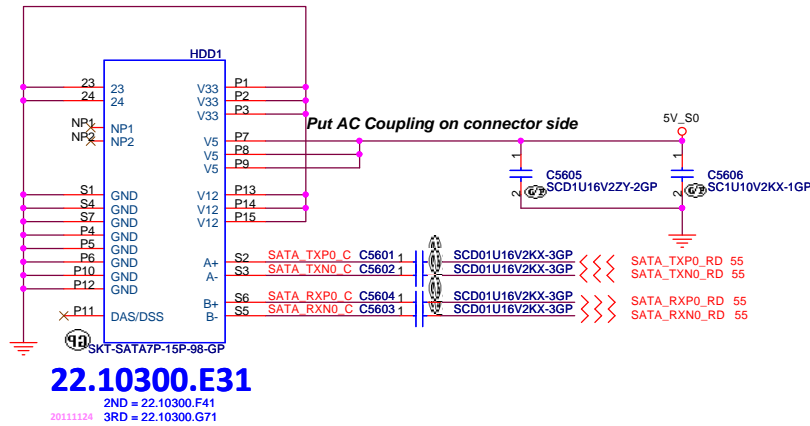


Please put under re-Driver IC bottom side.

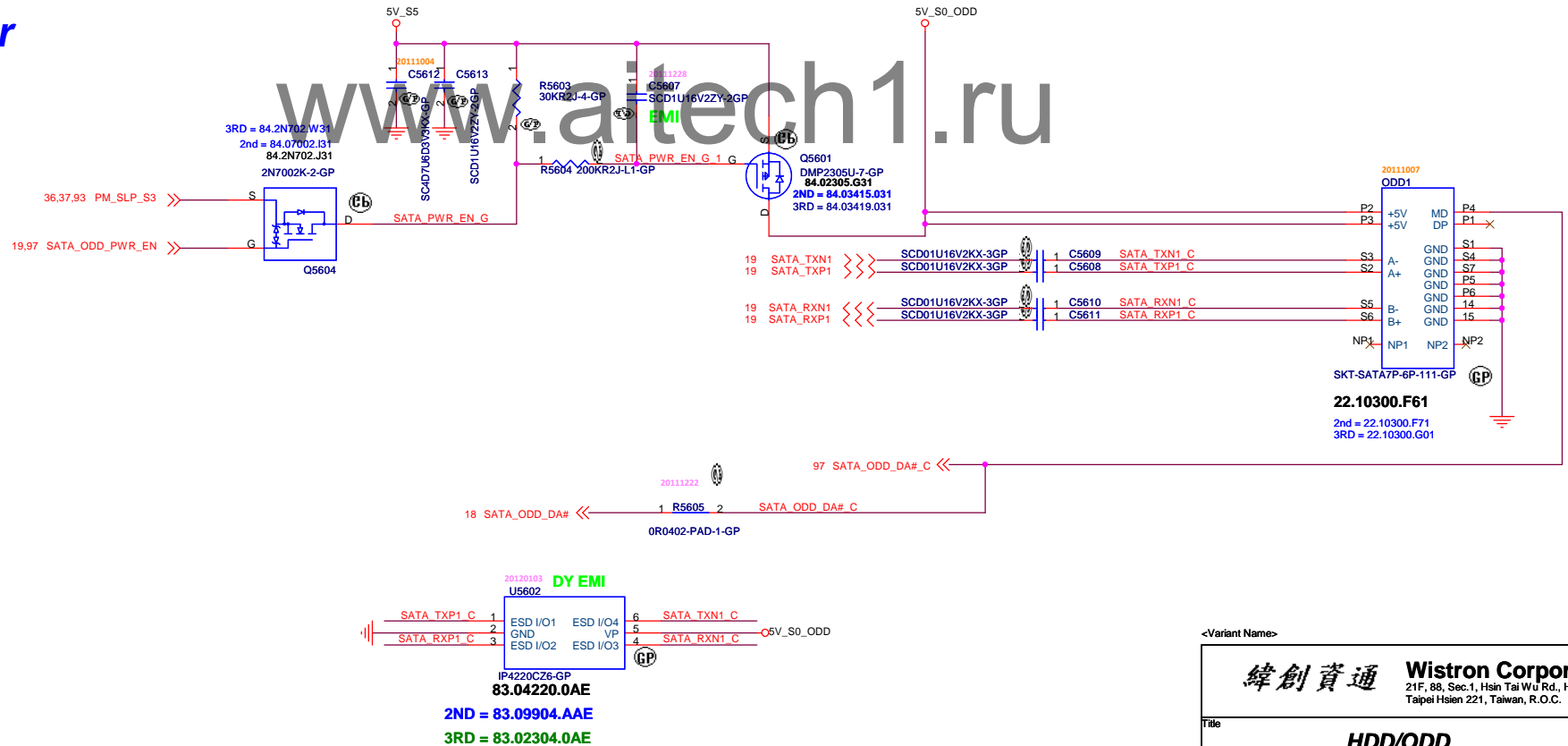
Configuration Table - Output Emphasis/Swing Setting

A_EM/B_EM	3 Gb/s	6 Gb/s
0	500mV pp	600mV pp
1	500mV pp + 3dB	600mV pp + 1.5dB

HDD Connector



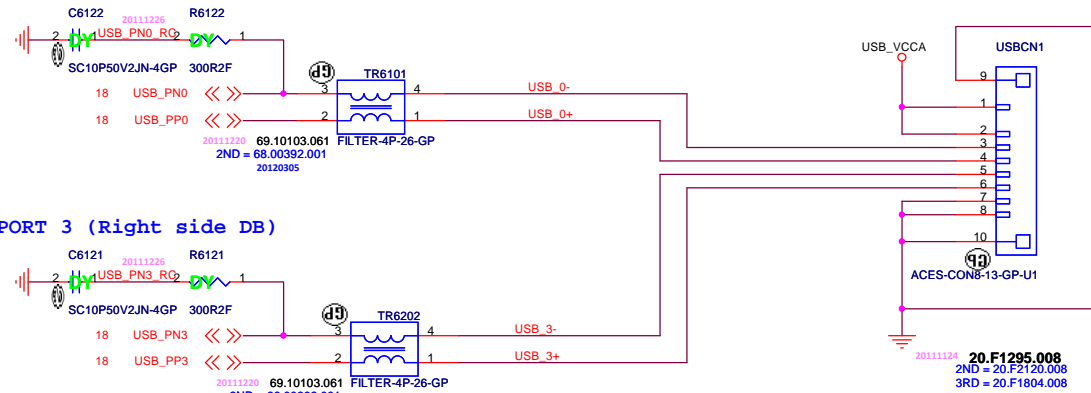
ODD Connector



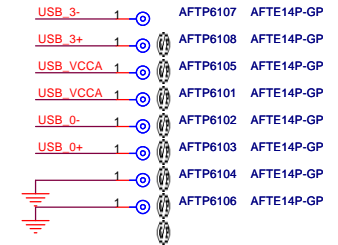
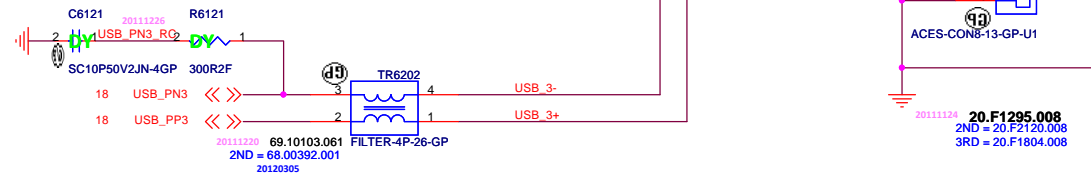
<Variant Name>

Right Side USB 2.0 Connector

USB 2.0 PORT 0 (Right side DB)

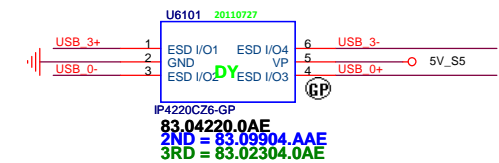
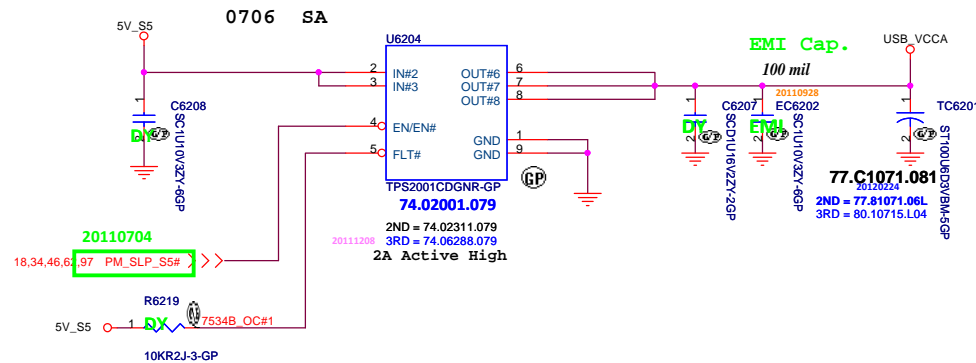


USB 2.0 PORT 3 (Right side DB)



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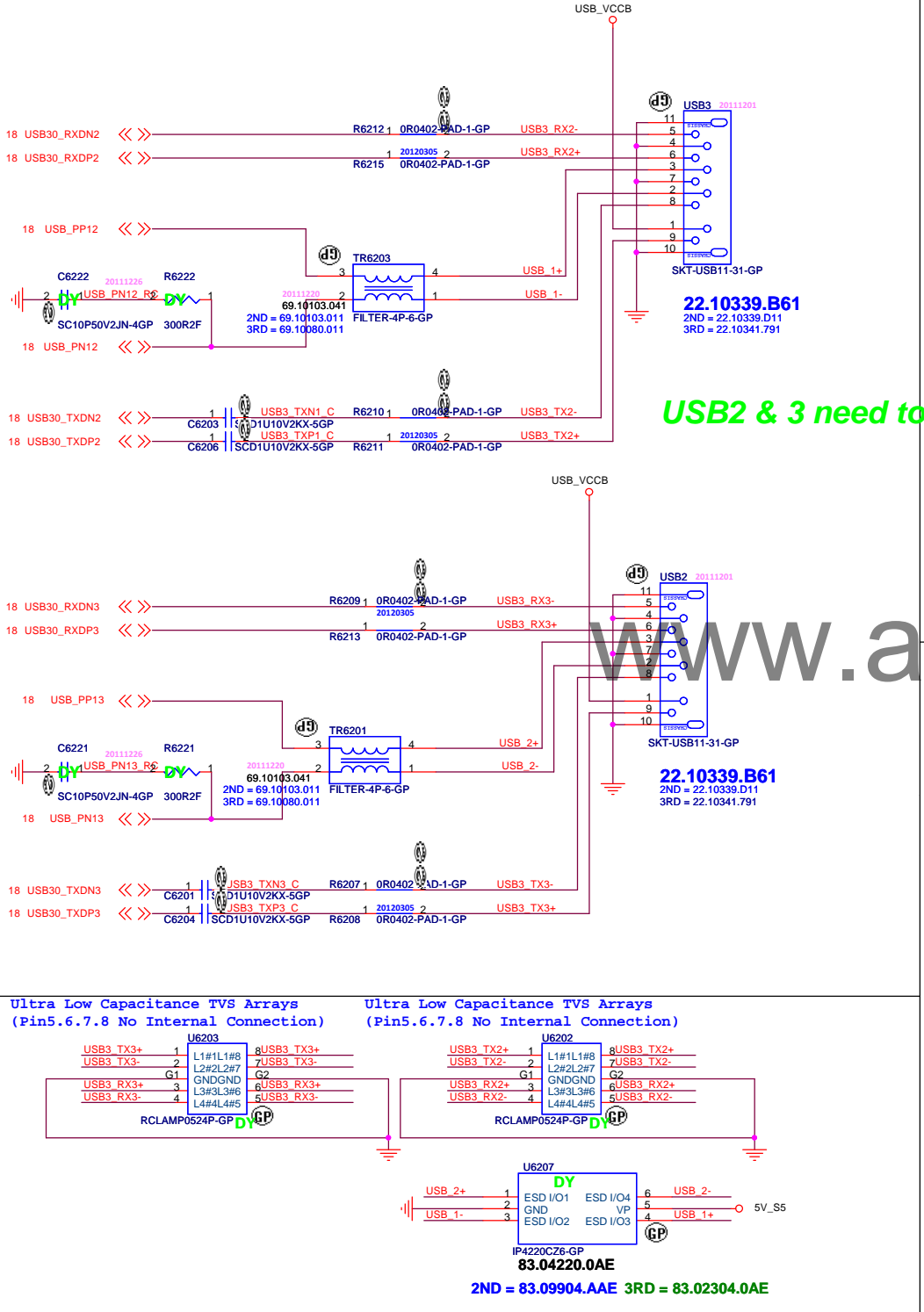
USB POWER



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB Power SW	
Title Size A3 Date: Monday, March 12, 2012	Document Number S series Popeye & Pebble SA Sheet 61 of 103

Left Side USB 3.0 Connector



USB 3.0 Connector
Pin definition

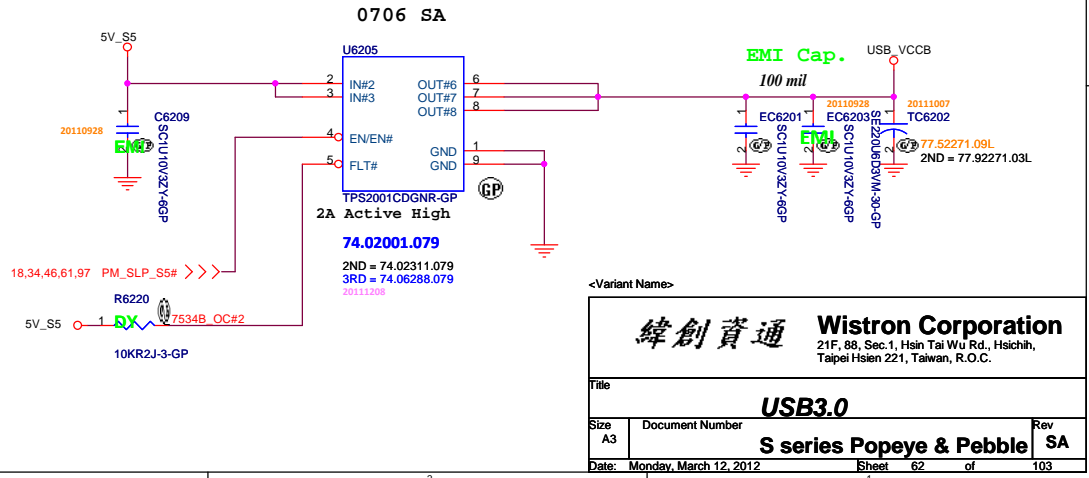
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

0622-2 SA

0706 SA Delete Test point

USB POWER

0622-2 SA



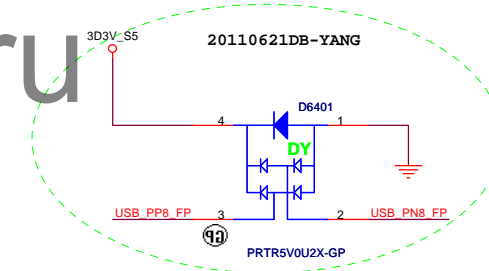
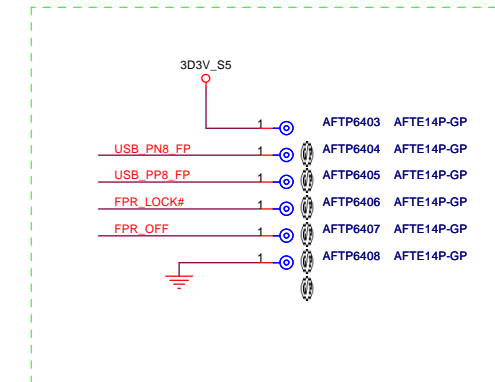
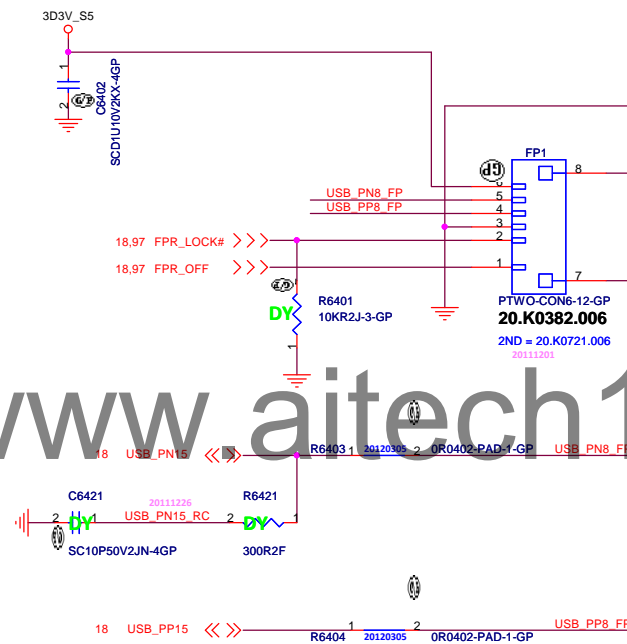
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

USB3.0

S series Popeye & Pebble

SA

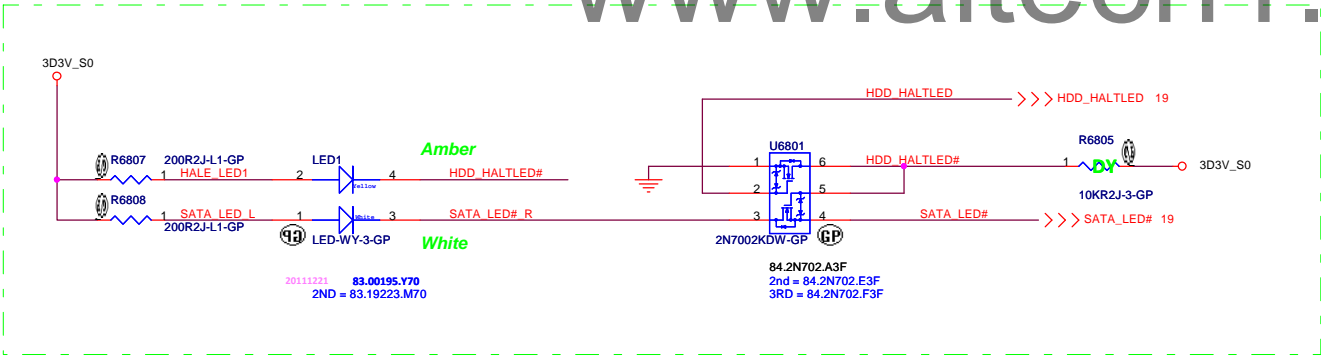
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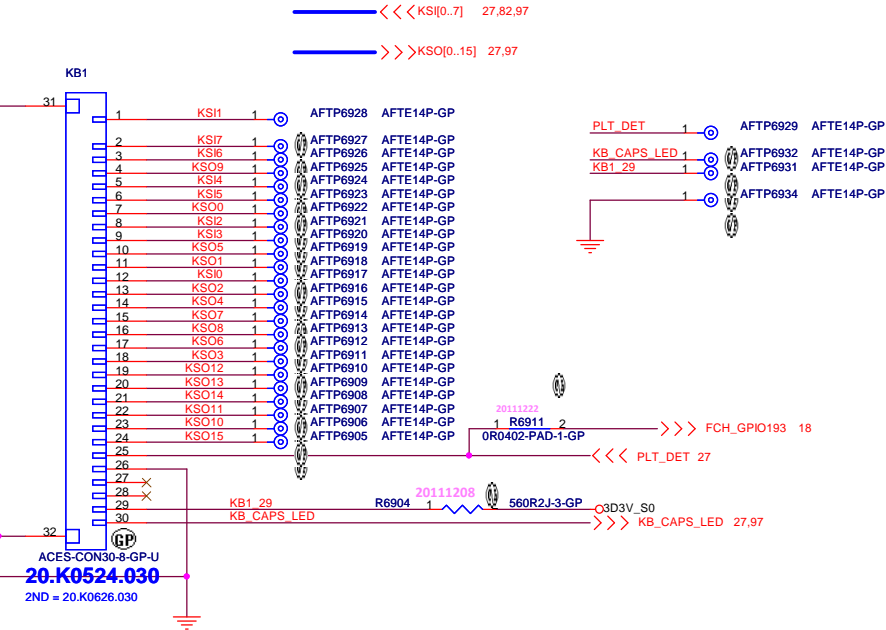
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		ACCELEROMETER	
Size A3	Document Number	S series Popeye & Pebble	Rev SA
Date:	Monday, March 12, 2012	Sheet 65	of 103

HDD LED



<Variant Name>

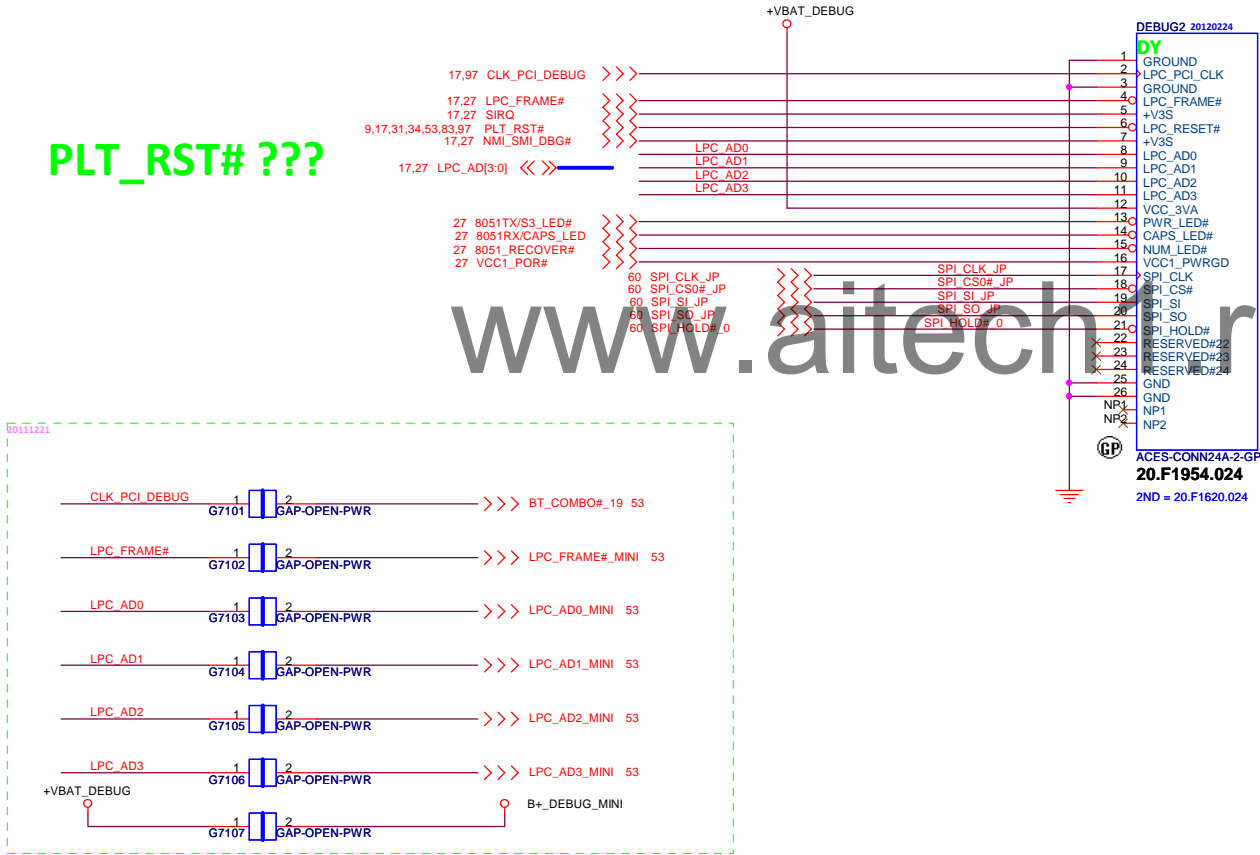
Keyboard Connector



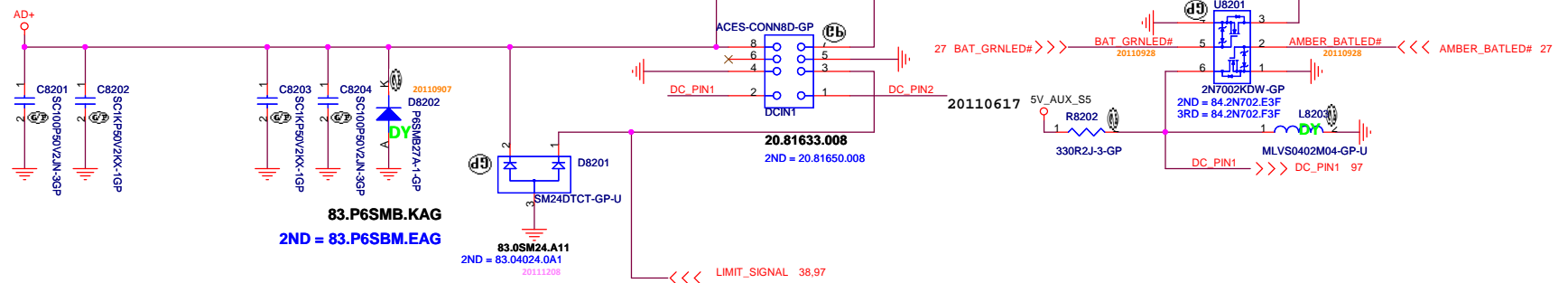
www.aitech1.ru

24 PIN LPC DEBUG CONN.

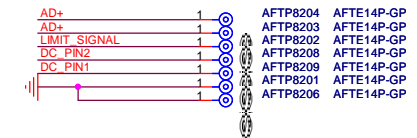
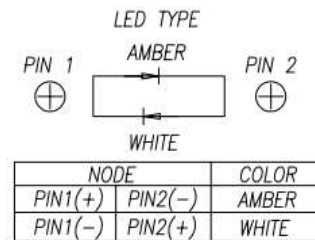
PLT_RST# ???



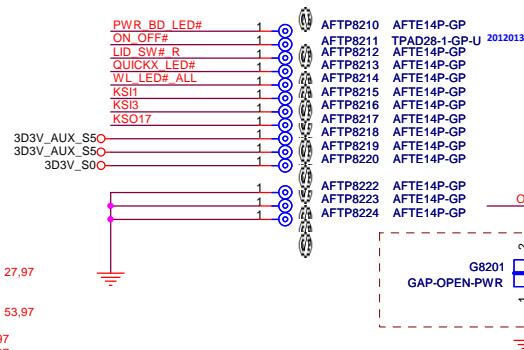
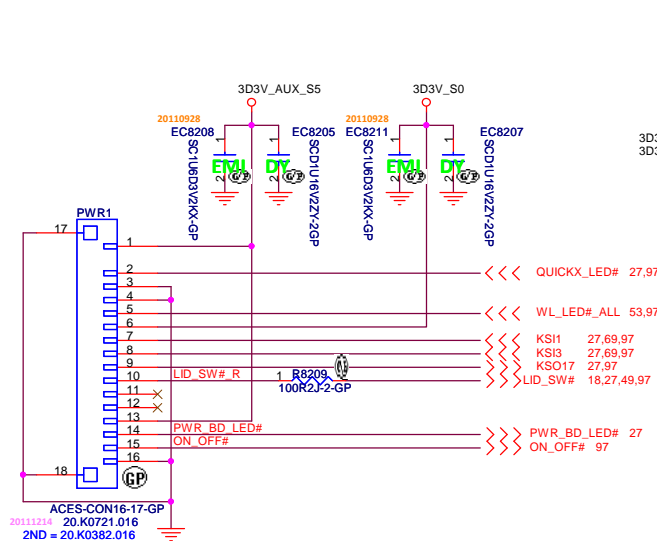
Adaptor in to generate DCBATOUT



	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low



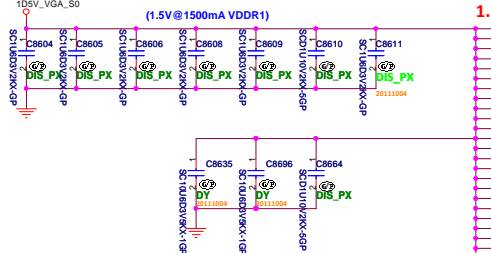
Power Button +Quick Lanch board



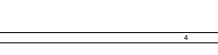
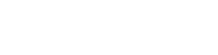
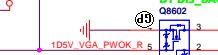
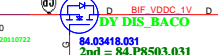
For layout: G8201
Under PWR1 and put on bottom side

dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DP[F:E]_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3, and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF

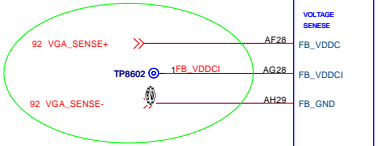
For DDR3/GDDR5, MVDDQ = 1.5V



120R @ 300mA

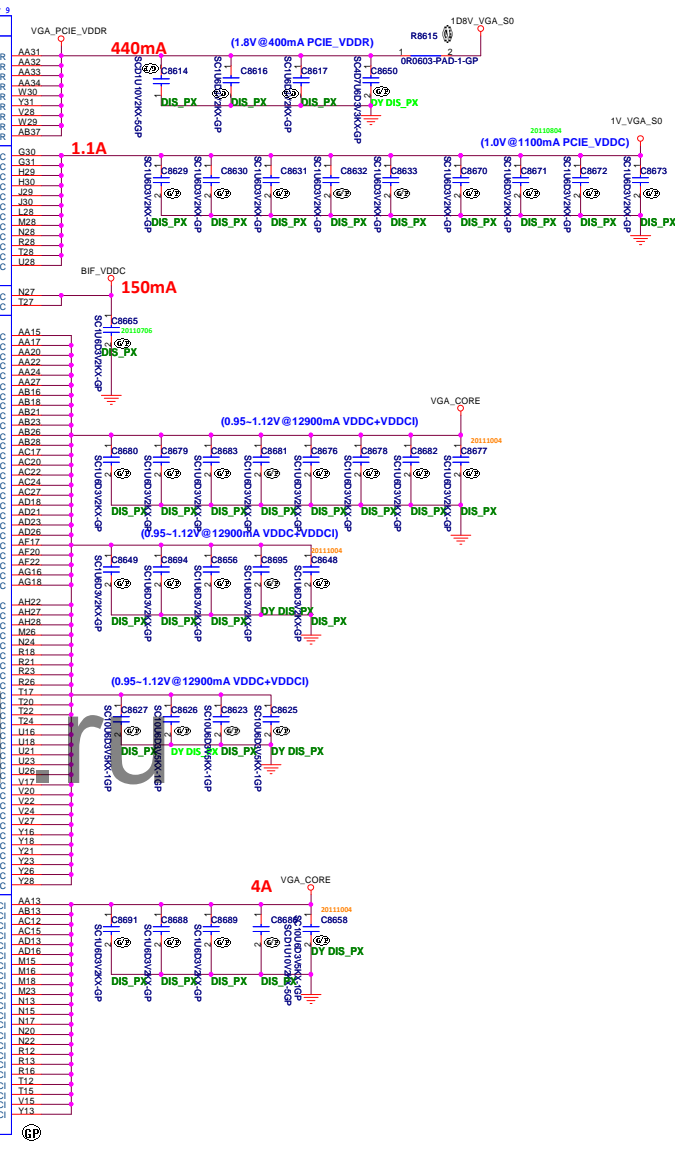


20110620



	PX_EN#	8209A_ENVDD_VGA1D5V_VGA_PWOK_R	PX_EN#	PX_EN#
Non-BACO	0	1	1	0
BACO	1	0	0	1

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN# = High, BIF_VDDC = VGA_CORE

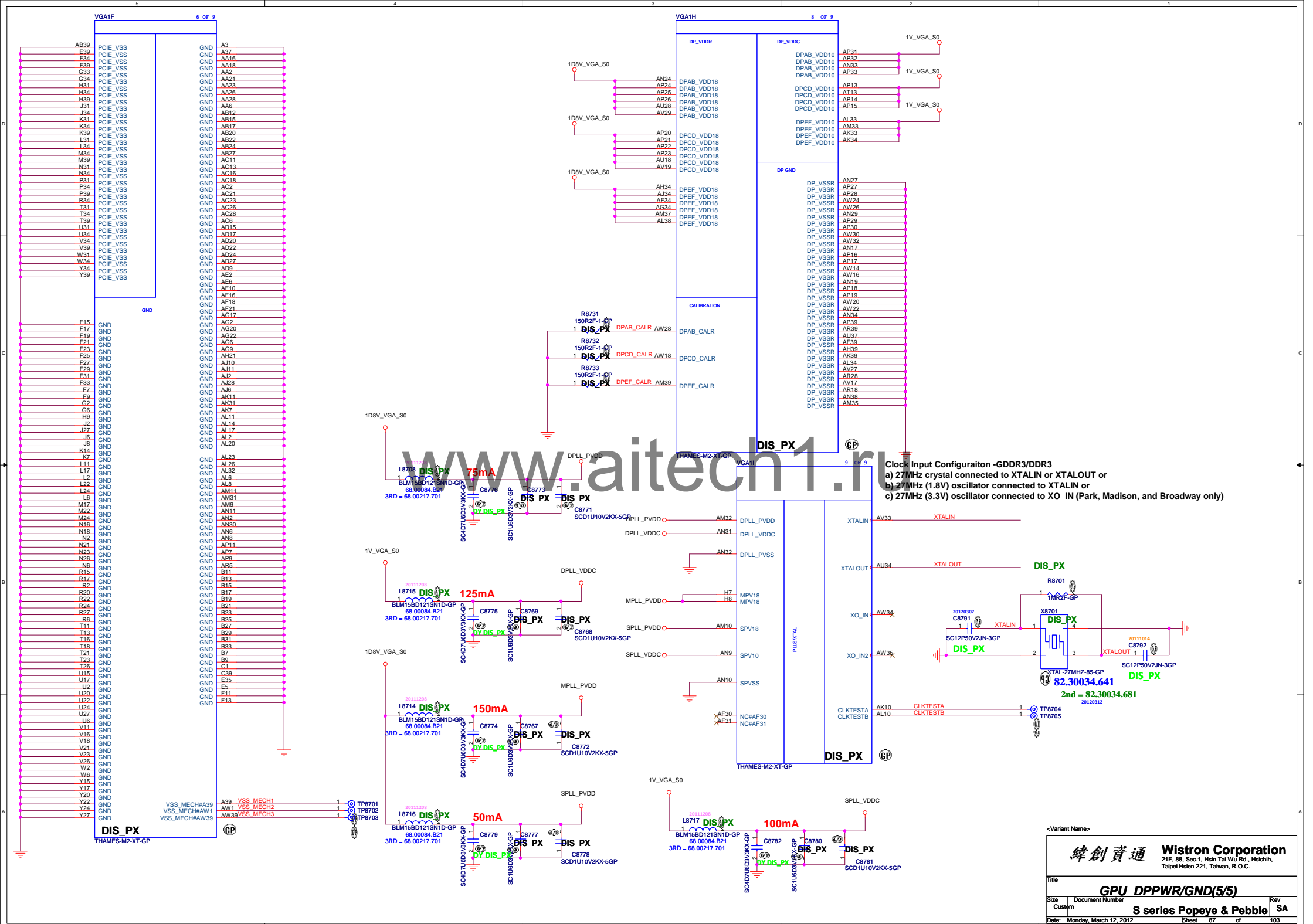


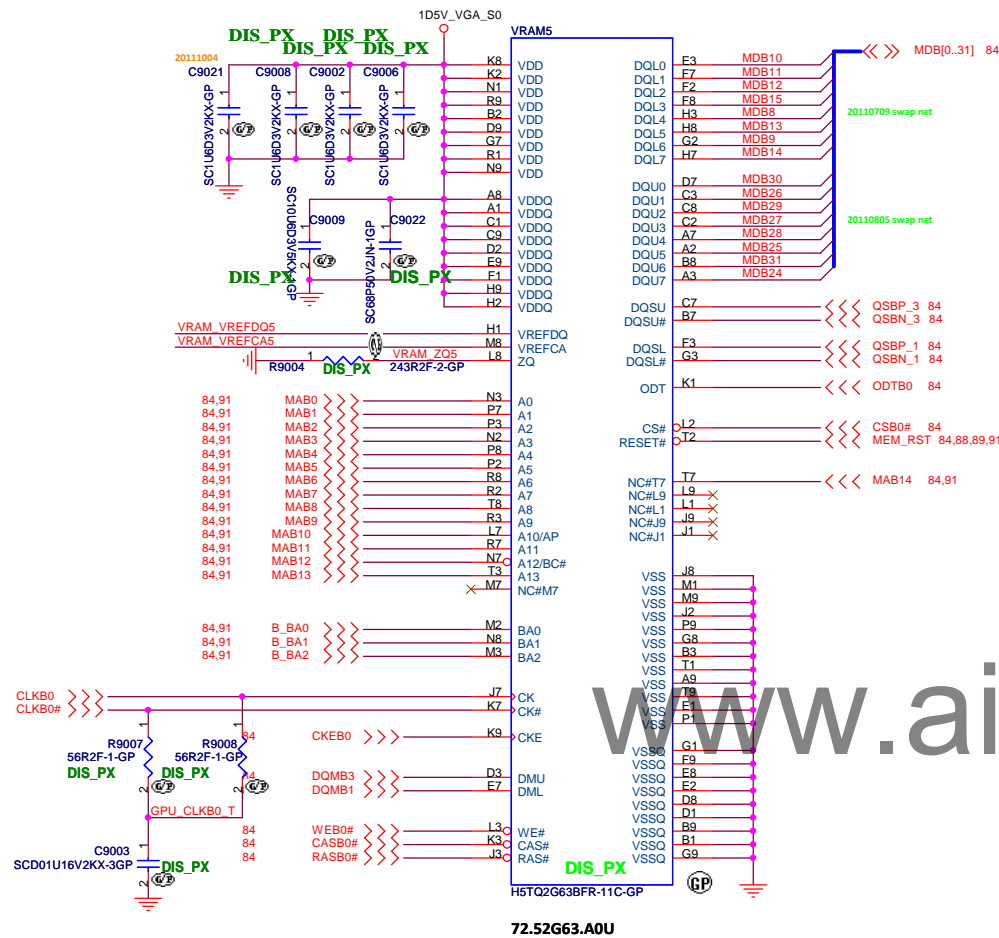
VGA_Core
1V_VGA_S0

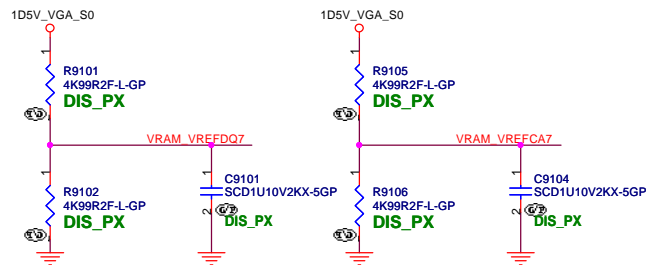
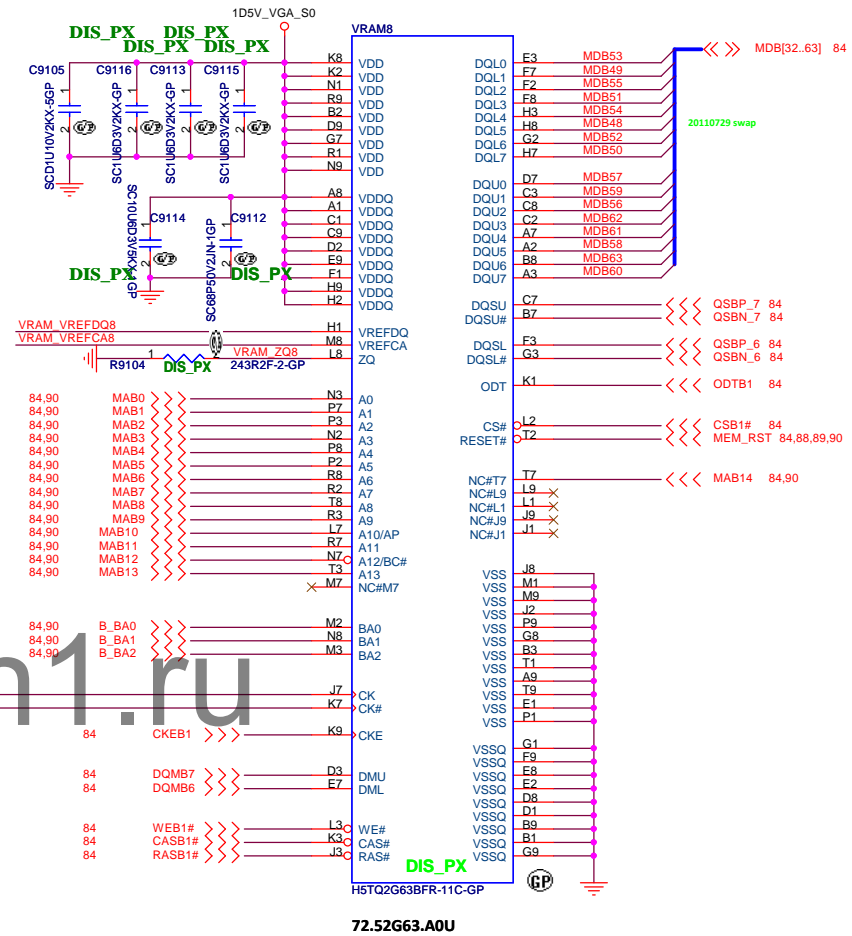
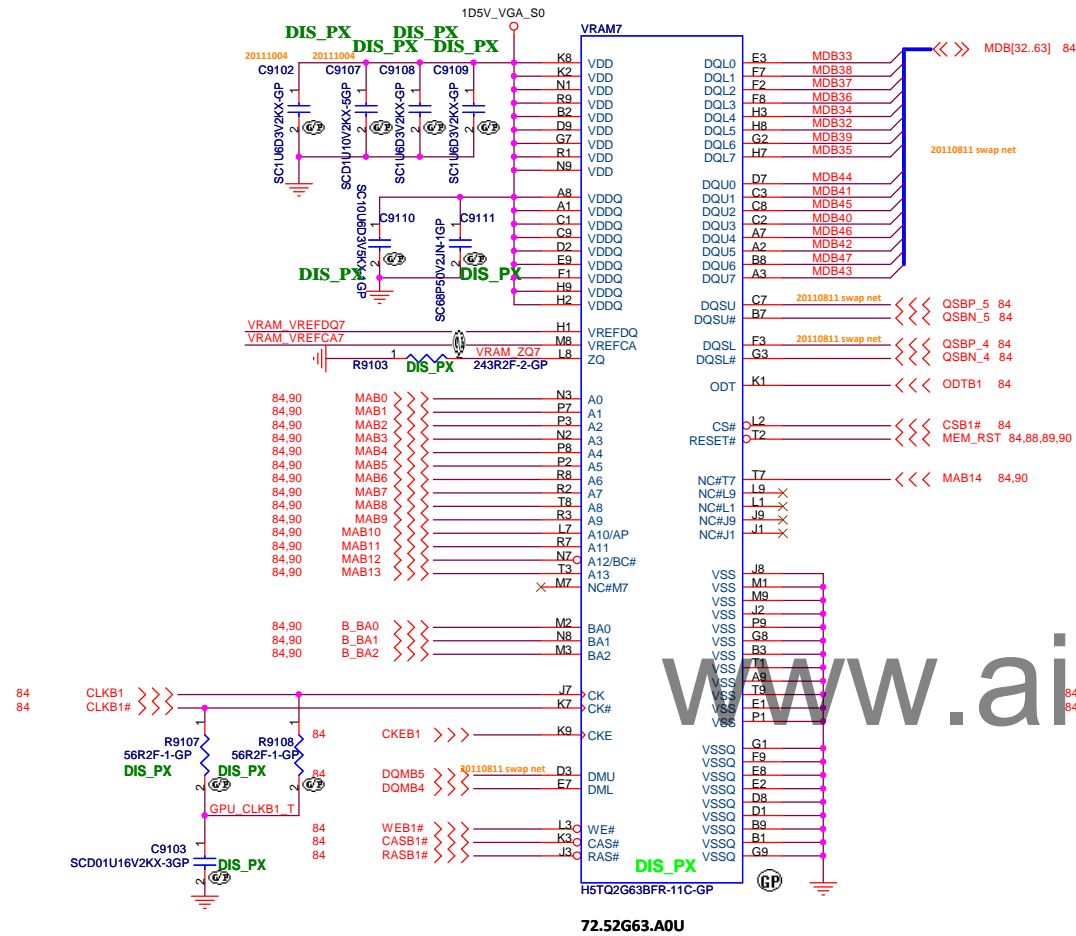
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

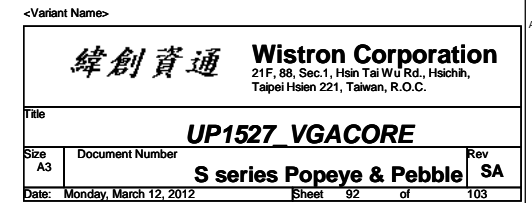
File: GPU_POWER(4/5)
Size: Document Number
Customer: S series Popeye & Pebble
Date: Monday, March 12, 2012 Sheet 86 of 103



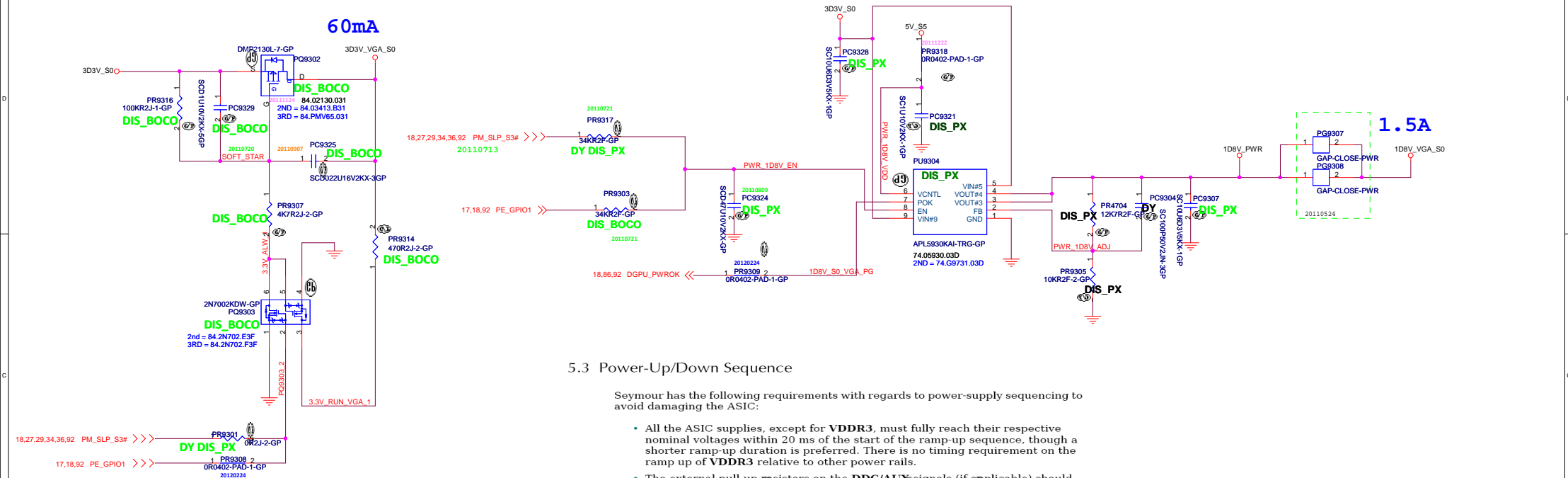




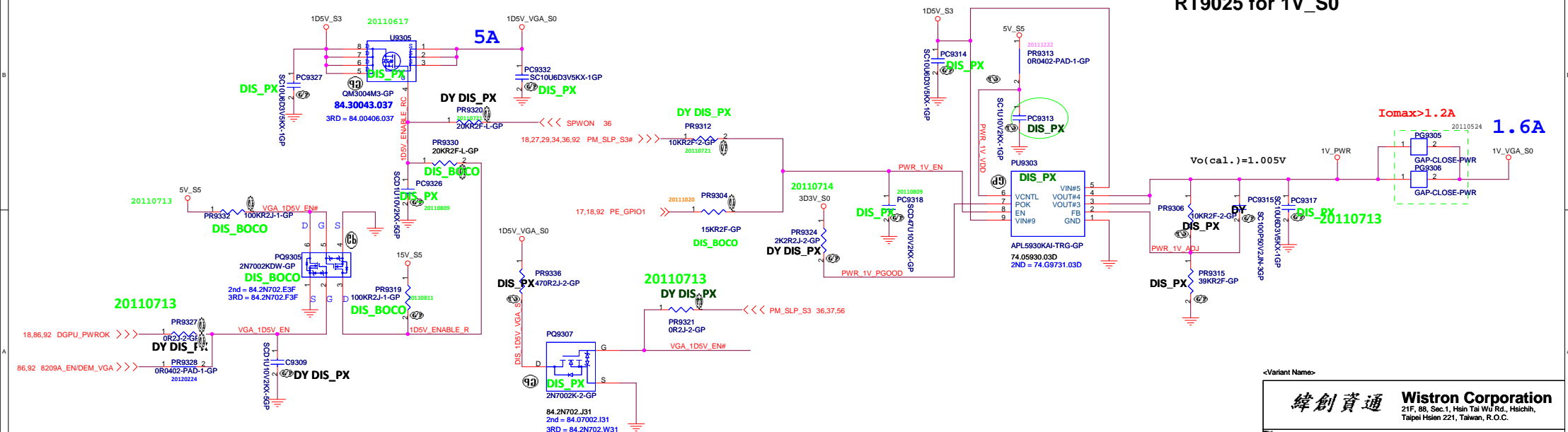
VDDC/VDDCI SCALING		
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VDDC/VDDCI
PWRCNTL_0	PWRCNTL_1	
0	0	1.0000
1	0	0.9000



3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



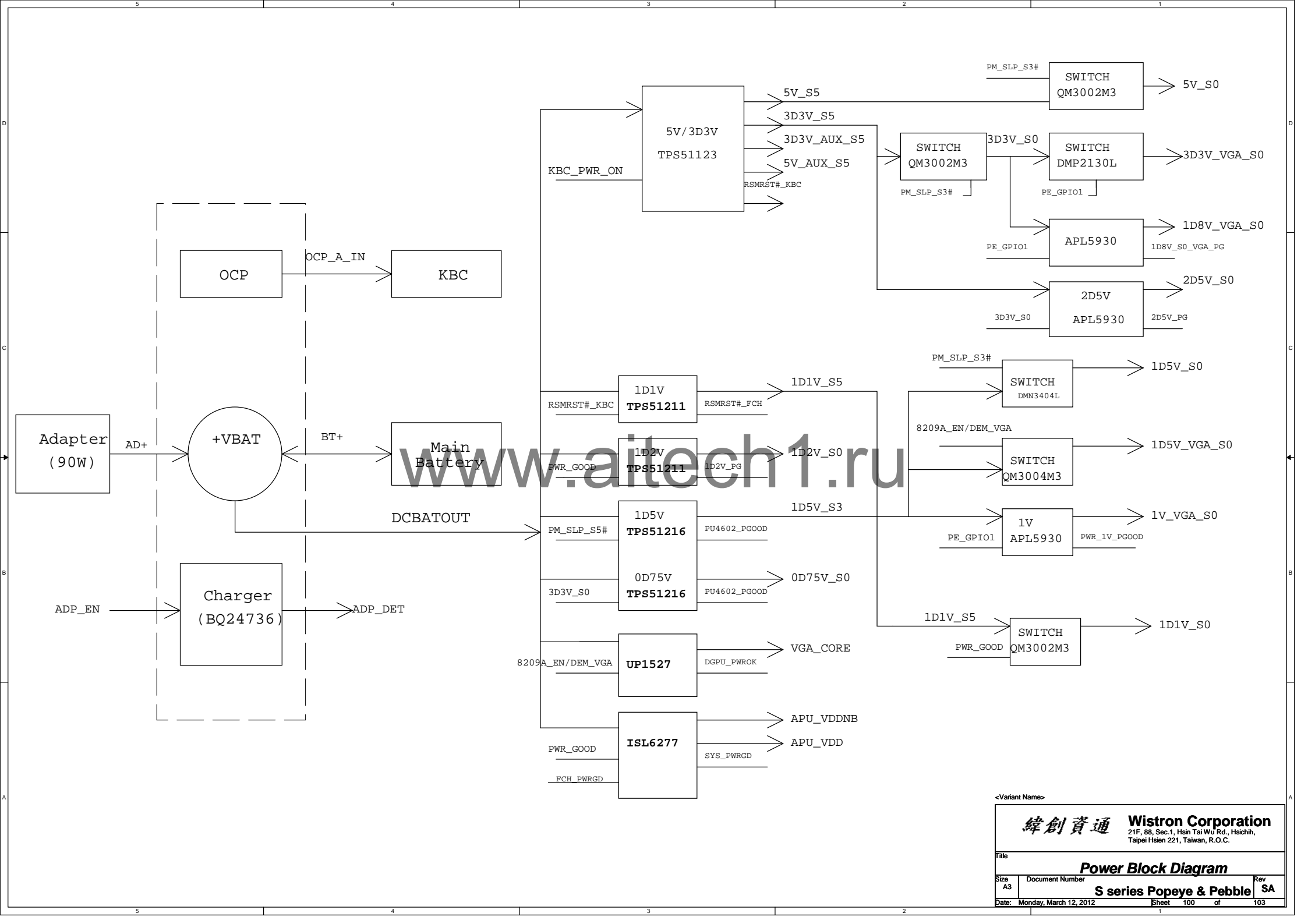
1D5V_VGA_S0



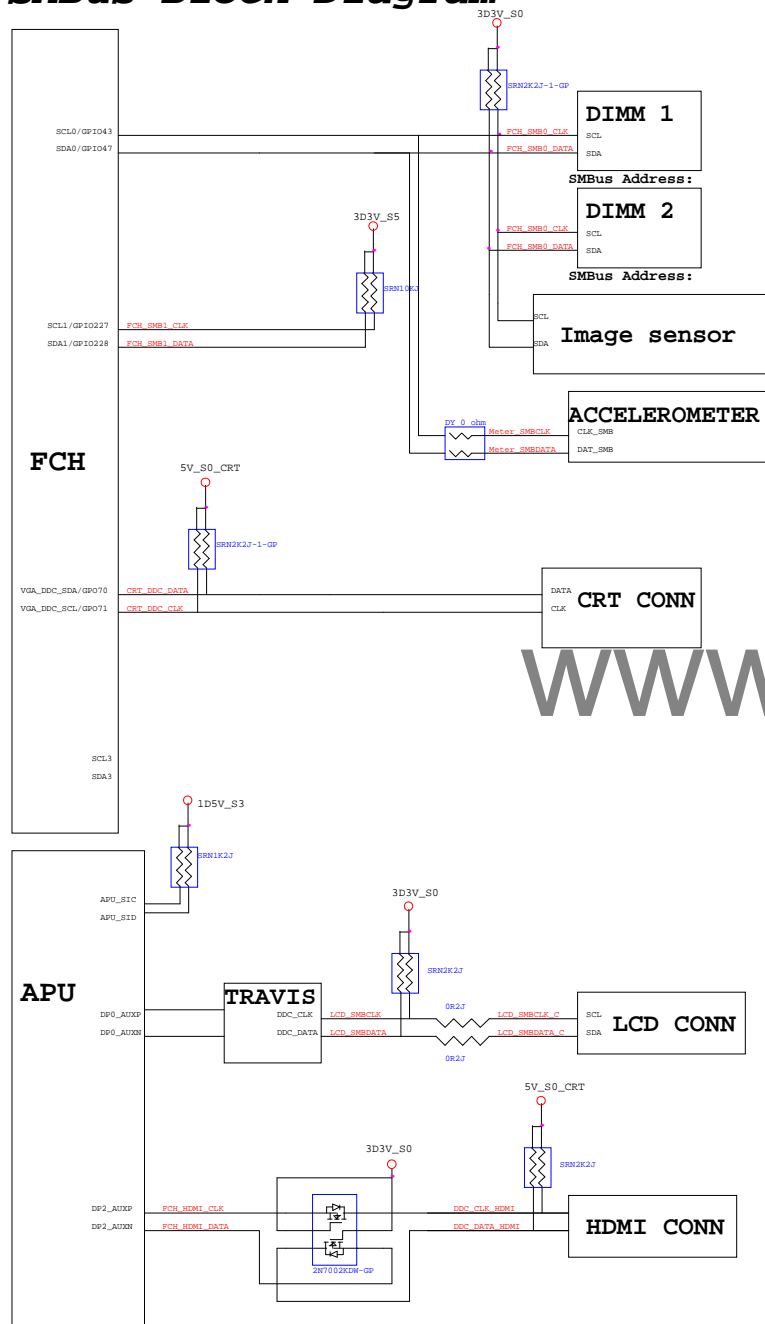
APU:
1. GROUP A(VDDIO,VDDA) ramp before GROUP B
(VDD RUN, VDDNB RUN, VDDP, VDDR)



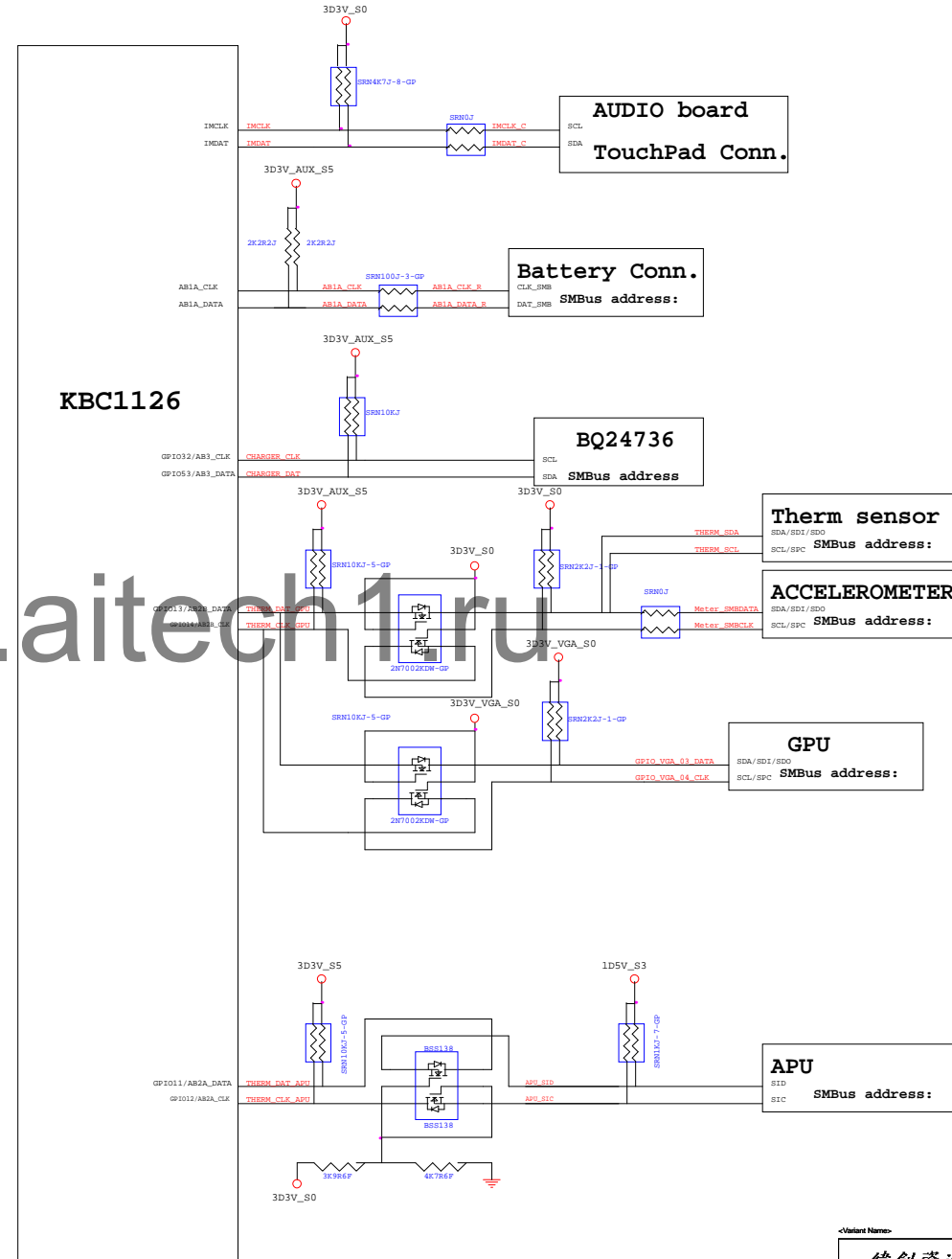
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Title	
<div> <div>Power Sequence</div> <div> <div>Size</div> <div>Document Number</div> <div>Rev</div> </div> <div> <div>Custom</div> <div>S series Popeye & Pebble</div> <div>SA</div> </div> </div>	
Date: Monday, March 12, 2012	File: 09_01_103



FCH SMBus Block Diagram



KBC SMBus Block Diagram

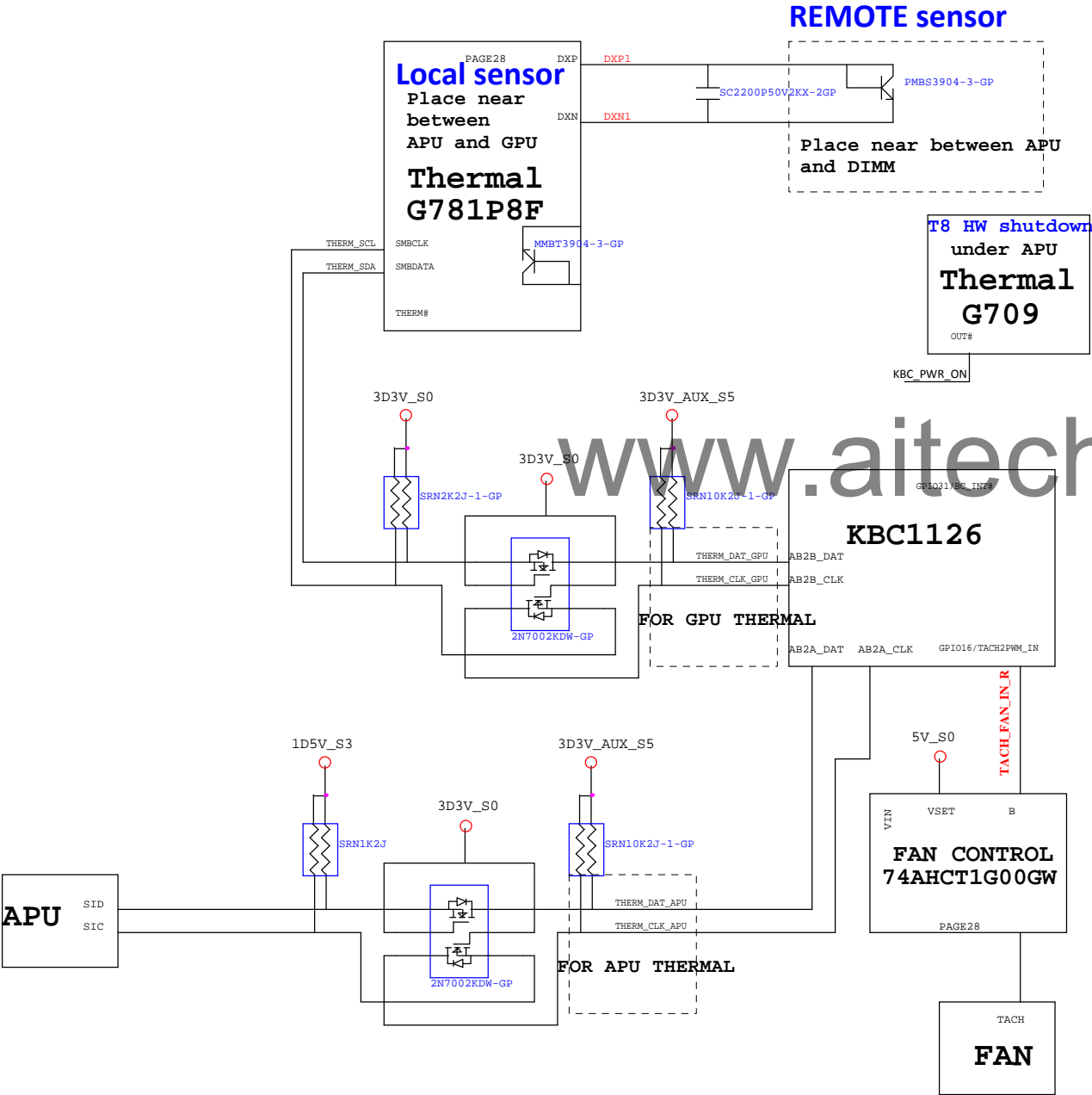


<Variant Name>

緯創資通 Wistron Corporation
2/F, 8th, Sec.1, Hsin-Tai Wu Rd., Hsinshui,
Taichung 411, Taiwan, R.O.C.

File
SMBUS Block Diagram
S series Popeye & Pebble SA
Date: Monday, March 12, 2012 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram

